ZYNQ UltraScale+ MPSOC ZU2_3_4_5 SOM User Manual



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Part 1: SOM Introduction

Part 1.1: SOM Introduction

The ZU2_3_4_5 SOM core board adopts the Zynq UltraScale+ 2/3/4/5 chip of XILINX company as the main controller. The core boards are completely compatible. The core board is designed to be compatible with the ZU2/3/4/5 chipset subdivision CG/EG/EV, and the carrier board design is fully compatible. The core board is connected to the carrier board with three 0.6mm pitch 120P gold-plated high-speed connectors, and four 3.5mm fixing holes are placed on the four feet of the core board. This hole can be fastened with the carrier board by screws, which ensures stable operation in the environment of strong vibration.

Part 1.2: SOM Specification

CR-ZU2/3/4/5 FPGA Board Resource				
FPGA CHIP	XCZU2CG-2SFVC784I	XCZU3EG-2SFVC784I	XCZU4EV-2SFVC784I	XCZU5EV-2SFVC784I
DDR4	PS-Side 4GB(2400Mhz*64bit)/PL-Side 1GB(2400Mhz*16bit)			
EMMC	8GB			
QSPI FLASH	32MB			
E2PROM	64Kbit			
UART/RS485/CAN	1 /1/1			
SD Card	1			
Gigabit Ethernet	PS-Side 1 / PL-Side 1			
Mini DP	1 (Supports up to 4K 30fps)			
RTC	1 in the core board/ Reserved 1RTC in the carrier board (not soldered)			
LED, Keys	5 LEDs (high level light up)、5 Keys (active in low level)			
SSD Memory	1（PS-Side, NVME）			
PCIE 3.0	--		2	
SFP	--		2	
40P expansion port	1, a total of 32 single-ended signals/16 pairs of differential signals			
120P expansion port	2, a total of 80 single-ended signals/40 pairs of differential signals			
Dimensions	Core Board: 83.8mm x 64.8mm, Carrier Board: 180mm x 122mm			
Board to Board Connectors	3 120P 0.6 high speed connectors, Height 3mm			
Operating Voltage	12V/3A			

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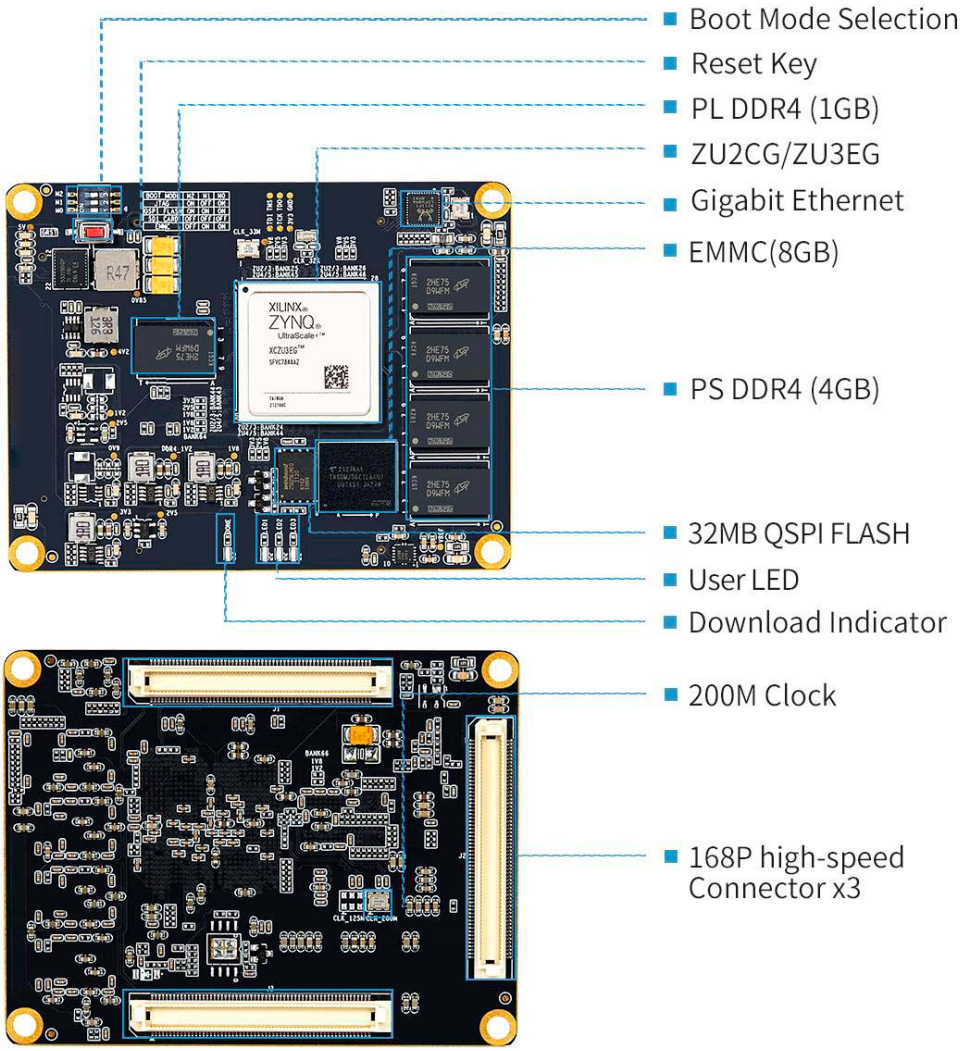
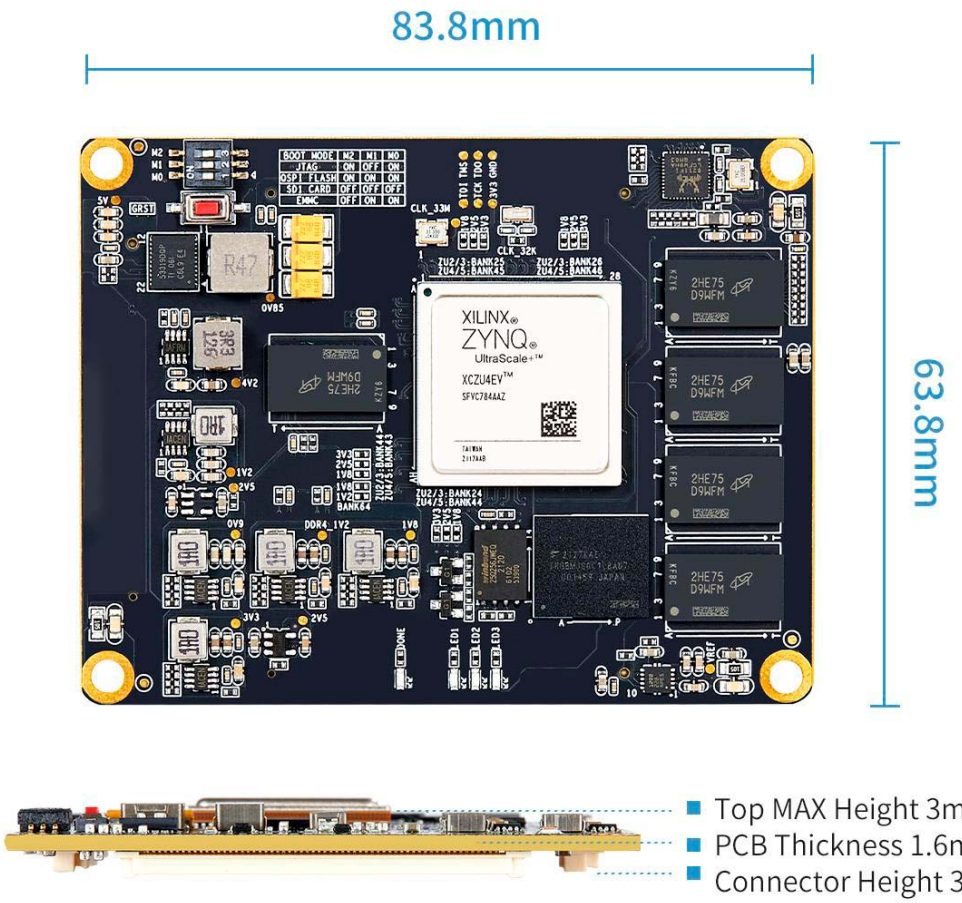
Part 1.3: Product Appearance

As shown in the figure below, the position of each main electronic component on the core board is marked, which is convenient for users to view and identify.



Part 1.4: SOM Form Factors

The Form Factors of the core board is 83.8 x 64.8mm. The core board is connected to the Carrier Board through three 0.6mm/120P gold-plated high-speed connectors on the bottom, with a combined height of 3mm. The following figure shows the dimensions of the core board.



Part 2: SOM User Guide

Part 2.1: Power Connection

The power supply voltage of the core board is 5V. There are power input pins on the four corners of the core board. The power pins have been connected inside the module. In the design, you only need to connect the power pin on one corner, and the core board can work. The power connection needs to be connected with copper and enough through holes are made to ensure the power flow capacity. All GND signals on the core board need to be connected to the carrier board, and each GND is connected to the carrier board through two vias. The limit current of the core board power supply is 5A/3A, so the external power supply needs to consider the limit

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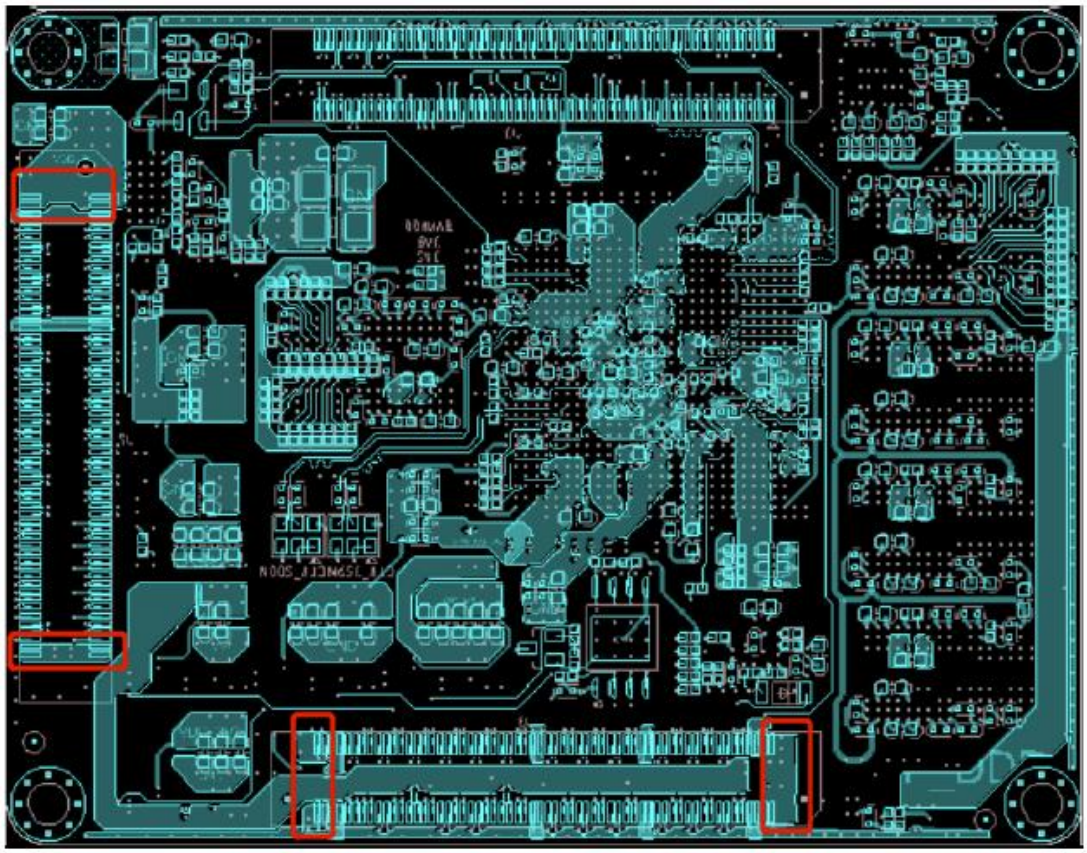
current to ensure the stable operation of the core board.

The output voltage of the power supply to the module needs to be stable. Add a first-level DCDC power conversion to the module power input, from high voltage to 5V, and the DCDC current output capacity can be about 5A. For example, you can refer to the power chip MP2482/MP2225. Two **220uF/25V** capacitors should be placed at the power input of the module to ensure power quality. If you are using tantalum capacitors, it is best to use a 1 ohm 0805 resistor in series with the capacitor to ensure the stability of the tantalum capacitor.



Part 2.2: Clock

The core board provides a 33.333Mhz clock input for the PS side, and the input pin position is PS_REF_CLK; it provides a 200Mhz differential clock input for the PL side. The clock input pins on the PL side is FPGA_12P_GC_65/FPGA_12N_GC_65, and the pin position is L3/L2; provides a 125Mhz differential clock input for the PL side GTX. Input position is GTX BANK224 CLK1, pin number is V6/V5

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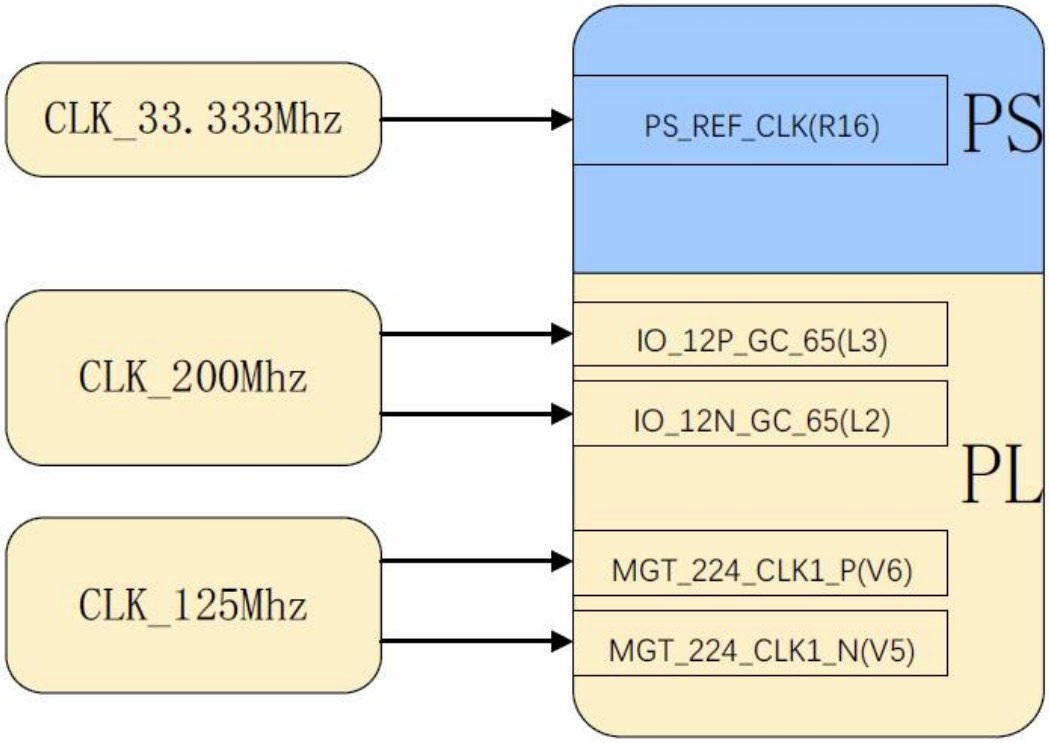

Part 2.3: Global Reset

The core board provides the "**nGST**" reset key, which is a system reset key and is active at low level. This pin is also drawn to the connector, and the signal name is "**SYS_nRST_I**", which is convenient for adding a reset key externally or designing a watchdog reset circuit. At the same time, in order to stabilize the system, we added a reset chip MAX811SEUS to the core board. The reset output signal is also led out to the connector, the signal name is SYS_nRST_O. This signal can be used for the reset of other peripherals on the core board. The signal level is 3.3V. The reset pin is a shared reset for PS/PL, which is connected to the PS_POR_500 (D21) pin on the PS side and the IO_L3N_34(G9) pin of the BANK44 on the PL side.

If the reset circuit needs to be designed on the carrier board, the following situations need to be considered.

1) The reset circuit board is used internally, only need to add a reset key and a 10uF capacitor parallel port to the ground.
2) The reset circuit needs to be reserved on the structure for external

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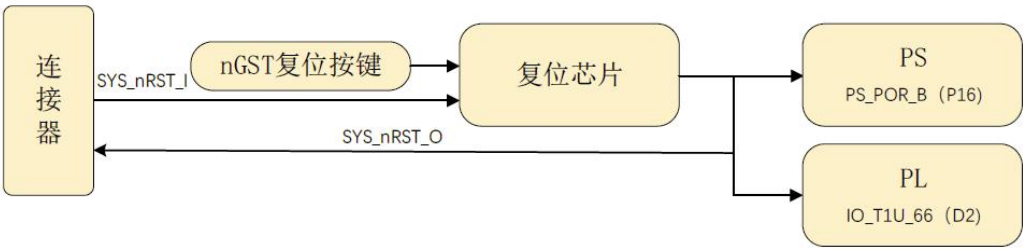
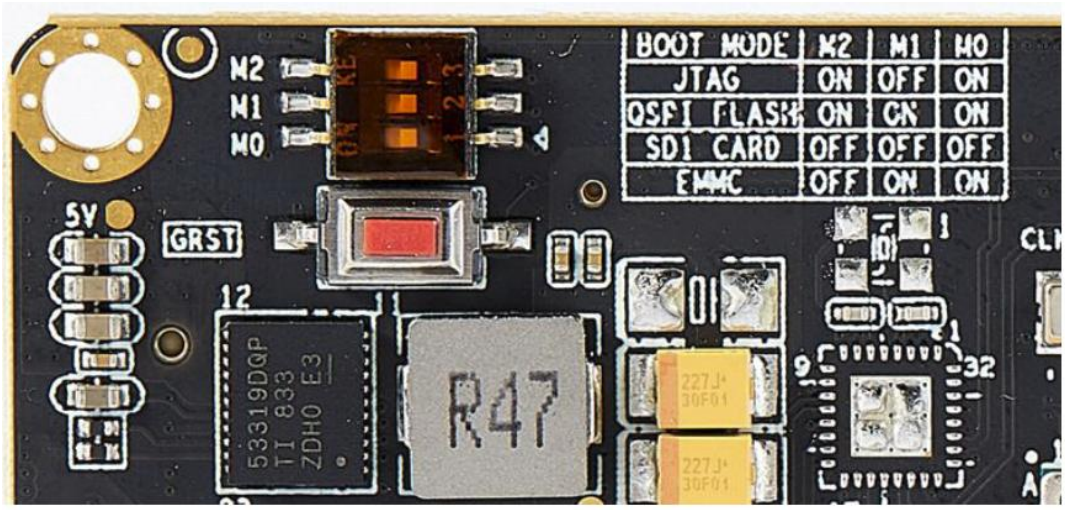
use. It is necessary to add a key to the ground, and at the same time, connect a 10uF capacitor and a TVS anti-static device to the ground in parallel.





Part 2.4: Boot Mode Selection

The core board supports four boot modes, namely JTAG, QSPI Flash, EMMC, and SD card. The first three startup methods are installed on the core board, and users can realize the SD card method by connecting with the carrier board. Four startup methods can be selected through the onboard DIP switch. The following figure has listed the position of each mode DIP switch. Because the main chip generates a large amount of heat, a heat sink needs to be added on the core board, which will block the BOOT MODE selection table.

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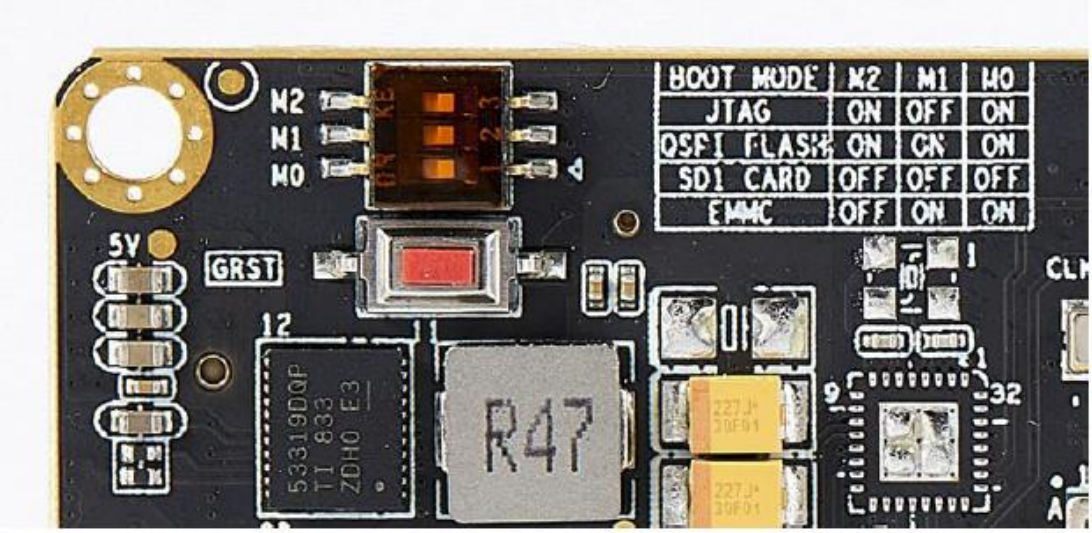

Part 2.5: Gigabit Ethernet Chip

The Gigabit Ethernet chip KSZ9031 is placed on the core board. The Ethernet chip and the ZYNQ chip are interconnected through the RGMII interface. The corresponding pins are shown in the table below. Ethernet external connection only needs an RJ45 with a transformer to use, the chip address PHY_AD[2:0]=001, the connection schematic diagram can refer to the following figure:

RMGII Signal	Pin Name	Pin Position
GTX_CLK	MIO26_501	L15
TXD0	MIO27_501	J15
TXD1	MIO28_501	K15
TXD2	MIO29_501	G16
TXD3	MIO30_501	F16
TX_EN	MIO31_501	H16
RX_CLK	MIO32_501	J16
RXD0	MIO33_501	L16
RXD1	MIO34_501	L17
RXD2	MIO35_501	H17
RXD3	MIO36_501	K17
RX_CTL	MIO37_501	J17
MDC	MIO76_502	B20
MDIO	MIO77_502	F20

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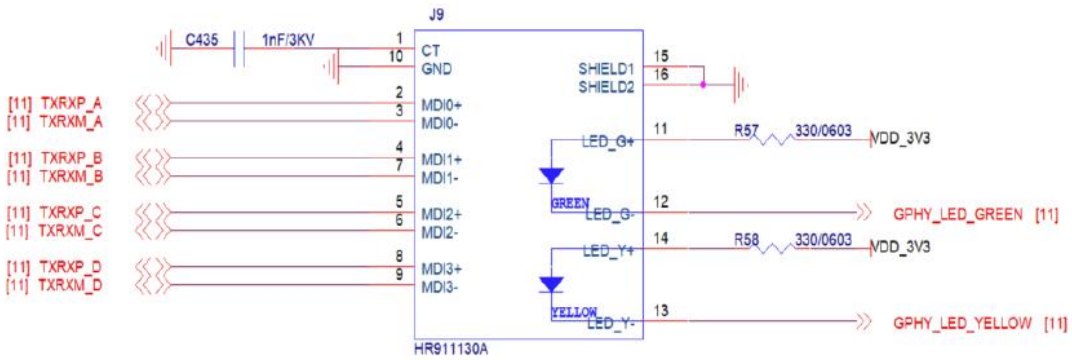

Part 2.6: EMMC Pin Definition

The onboard EMMC has a capacity of 8GB, and the module is THGBMFG6C1LBAIL, and the pin definitions are as follows.

EMMC Pin	Pin Name	Pin Position
EMMC_D0	MIO13	AH18
EMMC_D1	MIO14	AG18
EMMC_D2	MIO15	AE18
EMMC_D3	MIO16	AF18
EMMC_D4	MIO17	AC18
EMMC_D5	MIO18	AC19
EMMC_D6	MIO19	AE19
EMMC_D7	MIO20	AD19
EMMC_CLK	MIO22	AB20
EMMC_CMD	MIO21	AC21
EMMC_nRST	MIO23	AB18

Part 2.7: QSPI FLASH

Onboard 32 MB of QSPI FLASH, model MT25QU256ABA1EW9 0SIT, for storing boot files and user files

QSPI0 FLASH Pin	Pin Name	Pin Position
DATA0	MIO4	AH16
DATA1	MIO1	AG16
DATA2	MIO2	AF15
DATA3	MIO3	AH15
QSPI_CS	MIO5	AD16
QSPI_CLK	MIO0	AG15

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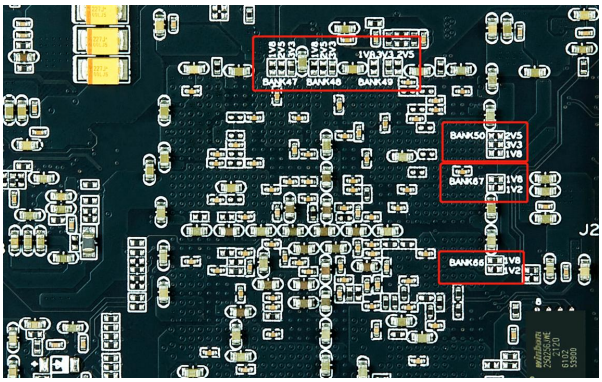
Part 2.8: On-board LED

In order to facilitate debugging, three LEDs are placed on the core board, and the LEDs are connected to the PL side. The pin positions of the LEDs are as shown in the table below. When the pin outputs a high level, the LED lights up, and the low level LED goes out.

Number	Pin Name	Pin Position
LED1	IO-T1U-64	AH6
LED2	IO-T2U-64	AB5
LED3	IO-T3U-64	AE4

Part 2.9: BANK Interface Level Selection

The BANK64/66 on the core board are HP BANK, the interface level is configured as 1.2/1.8V, and the voltage can be adjusted by 0 ohm resistance welding through the instructions provided on the single board, and the default level is 1.8V. BANK47/48/49/50 are HD BANK. Also for ZU2/3 and ZU4/5, the naming of HR BANK differs. For ZU2/3 that are BANK24/25/26/44. For ZU4/5, that are B ANK44/45/46/43, and the two BANKs correspond to each other and are pin compatible.BANK level can realize 1.8V/2.5V/3.3V three level conversion, just change the resistor position, the default level is 3.3V.



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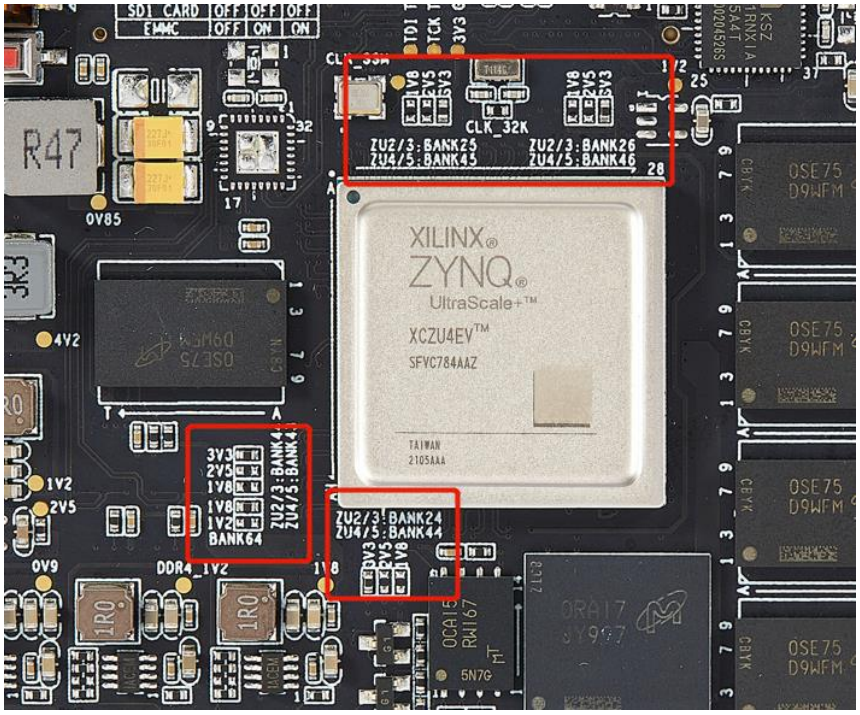

Part 2.10: PS-side DDR

The PS side is equipped with four industrial-grade DDR4 chips with a single capacity of 1GB and a total capacity of 4GB. The model is MT40A512M16LY-062E. The DDR4 pin assignment can directly call the system assignment. You can also refer to the routines provided by our company.

Part 2.11: PL-side DDR

The PL side is equipped with two industrial-grade DDR4 chips with a single capacity of 1GB, the model is MT40A512M16LY-062E, and the DDR4 pin assignment is shown in the table below.

DDR4 Pin	Pin Name	Pin Position
DDR4_D0	IO-L20P-65	J6
DDR4_D1	IO-L24P-65	H9
DDR4_D2	IO-L21P-65	J7
DDR4_D3	IO-L23P-65	K9
DDR4_D4	IO-L21N-65	H7
DDR4_D5	IO-L23N-65	J9
DDR4_D6	IO-L20N-65	H6
DDR4_D7	IO-L24N-65	H8
DDR4_DM0	IO-L19P-65	J5
DDR4_DQS_P0	IO-L22P-65	K8
DDR4_DQS_N0	IO-L22N-65	K7

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DDR4_D8	IO-L14P-65	M6
DDR4_D9	IO-L17N-65	N8
DDR4_D10	IO-L15N-65	N6
DDR4_D11	IO-L15P-65	N7
DDR4_D12	IO-L18N-65	L8
DDR4_D13	IO-L17P-65	N9
DDR4_D14	IO-L14N-65	L5
DDR4_D15	IO-L18P-65	M8
DDR4_DM1	IO-L13P-65	L7
DDR4_DQS_P1	IO-L16P-65	P7
DDR4_DQS_N1	IO-L16N-65	P6
DDR4_A0	IO-L8N-65	H1
DDR4_A1	IO-L3P-65	U8
DDR4_A2	IO-L8P-65	J1
DDR4_A3	IO-L3N-65	V8
DDR4_A4	IO-L11P-65	K4
DDR4_A5	IO-L4P-65	R8
DDR4_A6	IO-L9N-65	J2
DDR4_A7	IO-L2P-65	U9
DDR4_A8	IO-L9P-65	K2
DDR4_A9	IO-L1P-65	W8
DDR4_A10	IO-L4N-65	T8
DDR4_A11	IO-L7N-65	K1
DDR4_A12	IO-L6N-65	T6
DDR4_A13	IO-L1N-65	Y8
DDR4_A14	IO-L11N-65	K3
DDR4_A15	IO-L5P-65	R7
DDR4_A16	IO-T2U-65	P9
DDR4_BA0	IO-T1U-65	H2
DDR4_BA1	IO-L5N-65	T7
DDR4_BG0	IO-2N-65	V9
DDR4_CS	IO-L6P-65	R6
DDR4_nACT	IO-L13N-65	L6
DDR4_ODT	IO-L19N-65	J4
DDR4_RESET	IO-L7P-65	L1
DDR4_CLK_P	IO-L10P-65	H4
DDR4_CLK_N	IO-L10N-65	H3
DDR4_CKE	IO-T3U-65	K5
DDR4_A1	IO-L3P-65	U8
DDR4_A2	IO-L8P-65	J1
DDR4_A3	IO-L3N-65	V8
DDR4_A4	IO-L11P-65	K4
DDR4_A5	IO-L4P-65	R8
DDR4_A6	IO-L9N-65	J2
DDR4_A7	IO-L2P-65	U9
DDR4_A8	IO-L9P-65	K2
DDR4_A9	IO-L1P-65	W8
DDR4_A10	IO-L4N-65	T8
DDR4_A11	IO-L7N-65	K1
DDR4_A12	IO-L6N-65	T6
DDR4_A13	IO-L1N-65	Y8
DDR4_A14	IO-L11N-65	K3
DDR4_A15	IO-L5P-65	R7
DDR4_A16	IO-T2U-65	P9

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DDR4_BA0	IO-T1U-65	H2
DDR4_BA1	IO-L5N-65	T7
DDR4_BG0	IO-2N-65	V9
DDR4_CS	IO-L6P-65	R6
DDR4_nACT	IO-L13N-65	L6
DDR4_ODT	IO-L19N-65	J4
DDR4_RESET	IO-L7P-65	L1
DDR4_CLK_P	IO-L10P-65	H4
DDR4_CLK_N	IO-L10N-65	H3
DDR4_CKE	IO-T3U-65	K5

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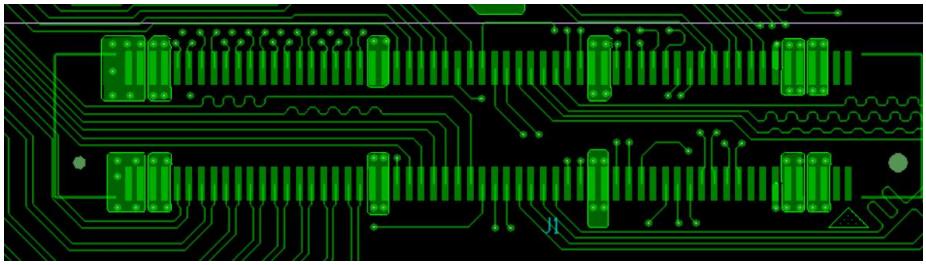
Part 3: Carrier Board Design

Part 3.1: PCB Design of Power Supply

The power input needs to be connected with copper skin, and enough vias are made to ensure the current carrying capacity, but the power supply voltage is high and the interference is large. Under the condition of ensuring the current flow, do not make the copper skin larger, so as not to interfere with other signals. The ground pins need to be connected to the ground plane, and one ground pin needs to be punched with two vias to ensure flow and sufficient connection.



Part 3.2: High-speed interface layout and routing

1) USB Interface

The parallel port rate of the USB PHY chip is 60Mhz, and the parallel port traces need to be equal in length and not greater than 1000mil (25.4mm), so the PHY should be placed as close to the module as possible, and the USB differential line DP/DM can be pulled longer.

2) Gigabit Ethernet

The signal connected to the RJ45 end needs to keep the same length, and the TX part and the RX part of the RGMII interface need to keep the same length separately.

3) HDMI Interface

The HDMI interface signal needs to be differential, and the same length control must be maintained between the differentials.

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Part 3.3: LVDS Signal

The BANK level of the core board can be selected between three levels of 1.2/1.8V/2.5V/3.3V, the default is 3.3V level, if you need to work in LVDS mode, you need to adjust the interface level to 1.8V or 2.5V. At the same time, the LVDS signal traces on the carrier board need to be processed by differential/impedance control, and the lengths between the differentials should be kept the same.

Part 3.4: GTX Signal Routing

There are many issues that need to be considered in GTX wiring. For users who have questions, contact customer service to access technical support.

Part 3.5: Product Protection

For product design, it is necessary to add protective circuits to various interfaces. It needs to be designed according to the requirements of the protection level.

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Part 4: SOM Core Board Pins and Signal Isometric

Part 4.1: SOM Core Board Pin Definition

The CR-ZU2/3/4/5 core board has a total of 38 pins on the PS side and 192 pins on the PL side. Among the PL pins, there are 96 signal levels of 1.2/1.8V, 96 signals can be adjusted at three levels of 1.8/2.5/3.3V. For detailed pin definitions, see the folder "ZU2/3/4/5 Core Board Pins Definition".

Part 4.2: Signal Isometric

In order to facilitate the user to design the carrier board and the high-speed signal, we provide the trace length data on the J1-J3 connectors to facilitate the user to coordinate the carrier board design. For the detailed data table, please refer to the folder "ZU2/3/4/5 Core Board Pins and Wire Length".

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