ZYNQ UltraScale+ MPSOC ZU2/3/4/5 FPGA Board User Manual

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Version Record:

Date	Version	Description
2021.02.13	V1.0	The first version

This tutorial will continue to be revised, optimized and added to the tutorial content based on actual development experience, providing you with more and better Demos, try out best to support you become an industry leader.

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Part 1: ZYNQ UltraScale+ MPSoC Introduction

The **Xilinx Zynq UltraScale MPSoC** architecture is based on **TSMC 16FinFET+** processing technology, enabling the next generation of **Zynq® UltraScale+ MPSoCs**. Building on the success of the **Zynq-7000 SoC** family, the new **UltraScale MPSoC** architecture further expands **Xilinx SoCs** to support true heterogeneous multiprocessing, providing the right engine for the right tasks in smarter systems, including:

- **Smarter Control**

  Interconnected Control Machine Room: Flexible/adaptable manufacturing, factory throughput, quality and safety

- **Smarter Vision**

  Advanced 2D/3D: Evolving video processing algorithms, object detection and analysis

- **Smarter Network**

  Wireless Communication: Supports multiple frequency bands and smart antennas

  Wired Communications: Multiple Wired Communications Standards and Context-Aware

  Network Services Data Center: Software Defined Networking (SDN), data preprocessing, and analytics

The **ZYNQ UltraScale MPSoC** architecture provides multiple advanced processors that scale from **32-bit** to **64-bit** with virtual support. **Xilinx** has been working with **ARM®** to provide the most efficient **64-bit ARMv8** application processor supporting **Cortex®-A53**, real-time low power coprocessor with **ARM® Cortex®-R5**, and **ARM® OpenGL ES 1.1/2.0** compliant **Mali™-400MP multi-core GPU**, leveraging ARM's leadership in embedded processors and its ecosystem. In addition, the **ZYNQ UltraScale MPSoC** also includes an **H.265/H.264** video codec unit that provides native **UltraHD** compression and a dedicated engine for dynamic power management and security configuration requirements.

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Xilinx has a variety of tools to support the benefits of **SoC**s, offering the **Vivado® Design Suite**, **Xilinx SDK**, and **PetaLinux** to further accelerate development using the **SDx™** family of design abstraction environments to efficiently leverage the power of the **ZYNQ UltraScale+ MPSoC**. The basic elements of this architecture include:

- 64-bit quad-core ARM Cortex-A53 processor
- Dual core ARM Cortex-R5
- Real-time processor ARM Mali™-400MP
- Graphics processor H.265/264
- Video codec unit
- Advanced Dynamic Power Management Unit
- Configure security cells
- DDR4/LPDDR4 memory interface support
- 16FinFET+ unit power performance
- SDSoC development environment (design abstraction)
- Next Generation AXI Interconnect

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Part 2: FPGA Board Overview

Part 2.1: FPGA Board Introduction

Cruetech's ZYNQ UltraScale+ MPSOC family FPGA development board has made four compatible versions ZU2/3/4/5. For ZU2/ZU3 two platforms, because the chip does not have a GTX high-speed interface, there is no SFP/PCIE on the FPGA development board. interface. For the ZU4/ZU5 two platforms, the chip has a GTX high-speed interface, so the FPGA development board has an SFP/PCIE interface. All four platforms are fully compatible with other peripherals.

Cruetech ZYNQ UltraScale+ family FPGA development board is provided in the form of core board and carrier board. The core board is fastened to the carrier board through three 120P high-speed connectors, which is more flexible in use. It can be used for learning, or the core board can be used for project development.

The FPGA development board integrates rich peripheral resources and provides detailed development routines. In addition, the FPGA development board also integrates a JTAG debugger, a MicroUSB cable and a 12V power adapter can make the development board work, making it more convenient for users to use.

The form factors of the FPGA development board is 180mmx122mm, and a fixing hole is placed at each of the four corners of the FPGA board to install the support column or fix the board, and the hole diameter is 3.5mm. The following is the specification of FPGA core board and it’s carrier board.

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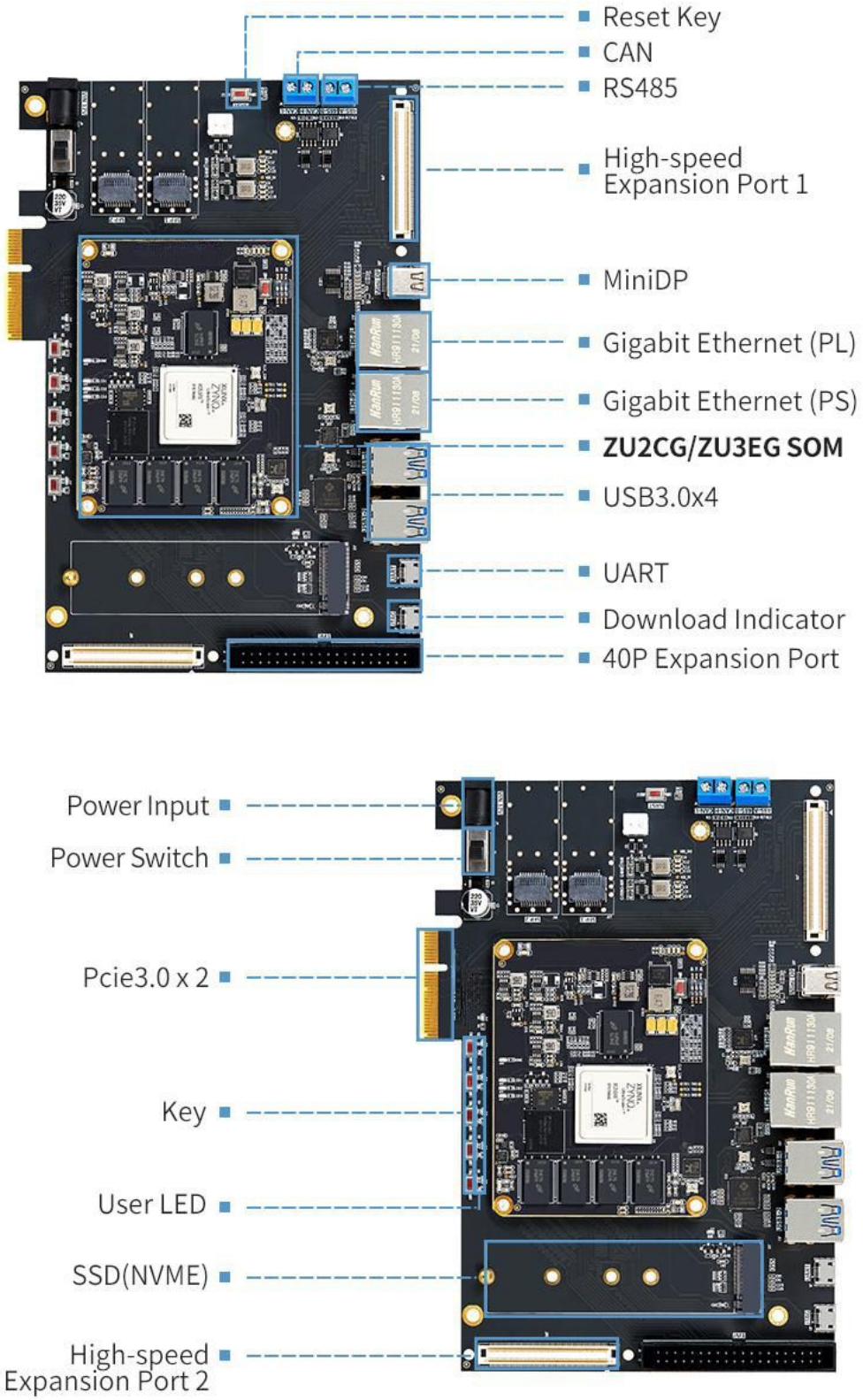

Figure 2-1-1: FPGA Board Specification

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Part 2.2: FPGA Board Resources and Block Diagram

The onboard resources of the FPGA development board are listed in the following table and block diagram, and all the functions included in the platform can be seen from the table below.

CRZU2/3/4/5B FPGA Board Resource				
FPGA CHIP	XCZU2CG-2SFVC784I	XCZU3EG-2SFVC784I	XCZU4EV-2SFVC784I	XCZU5EV-2SFVC784I
DDR4	PS-Side 4GB(2400Mhz*64bit)/PL-Side 1GB(2400Mhz*16bit)			
EMMC	8GB			
QSPI FLASH	32MB			
E2PROM	64Kbit			
UART/RS485/CAN	1 /1/1			
SD Card	1			
Gigabit Ethernet	PS-Side 1 / PL-Side 1			
Mini DP	1 (Supports up to 4K 30fps)			
RTC	1 in the core board/ Reserved 1RTC in the carrier board (not soldered)			
LED, Keys	5 LEDs (high level light up)、5 Keys (active in low level)			
SSD Memory	1（PS-Side, NVME）			
PCIE 3.0	--		2	
SFP	--		2	
40P expansion port	1, a total of 32 single-ended signals/16 pairs of differential signals			
120P expansion port	2, a total of 80 single-ended signals/40 pairs of differential signals			
Dimensions	Core Board: 83.8mm x 64.8mm, Carrier Board: 180mm x 122mm			
Board to Board Connectors	3 120P 0.6 high speed connectors, Height 3mm			
Operating Voltage	12V/3A			

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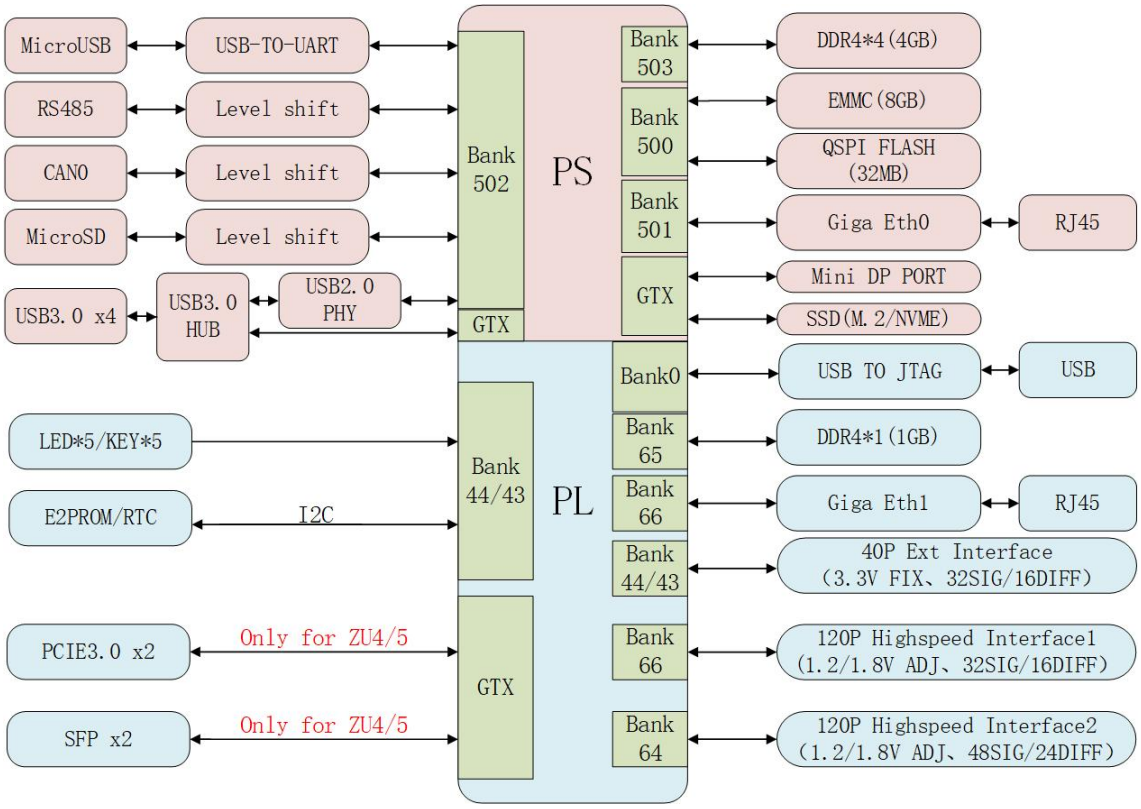

Figure 2-2-1: FPGA Board Block Diagram

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Part 3: SOM Introduction

Part 3.1: SOM Introduction

The ZU2_3_4_5 SOM core board adopts the Zynq UltraScale+ 2/3/4/5 chip of XILINX company as the main controller. The core boards are completely compatible. The core board is designed to be compatible with the Z U2/3/4/5 chipset subdivision CG/ E G/EV, and the carrier board design is fully compatible. The core board is connected to the carrier board with three 0.6mm pitch 120P gold-plated high-speed connectors, and four 3.5mm fixing holes are placed on the four feet of the core board. This hole can be fastened with the carrier board by screws, which ensures stable operation in the environment of strong vibration.

Part 3.2: SOM Specification

CRZU2/3/4/5C FPGA Board Resource				
FPGA CHIP	XCZU2CG-2SFVC784I	XCZU3EG-2SFVC784I	XCZU4EV-2SFVC784I	XCZU5EV-2SFVC784I
DDR4	PS-Side 4GB(2400Mhz*64bit)/PL-Side 1GB(2400Mhz*16bit)			
EMMC	8GB			
QSPI FLASH	32MB			
E2PROM	64Kbit			
UART/RS485/CAN	1 /1/1			
SD Card	1			
Gigabit Ethernet	PS-Side 1 / PL-Side 1			
Mini DP	1 (Supports up to 4K 30fps)			
RTC	1 in the core board/ Reserved 1RTC in the carrier board (not soldered)			
LED, Keys	5 LEDs (high level light up)、5 Keys (active in low level)			
SSD Memory	1（PS-Side, NVME）			
PCIE 3.0	--		2	
SFP	--		2	

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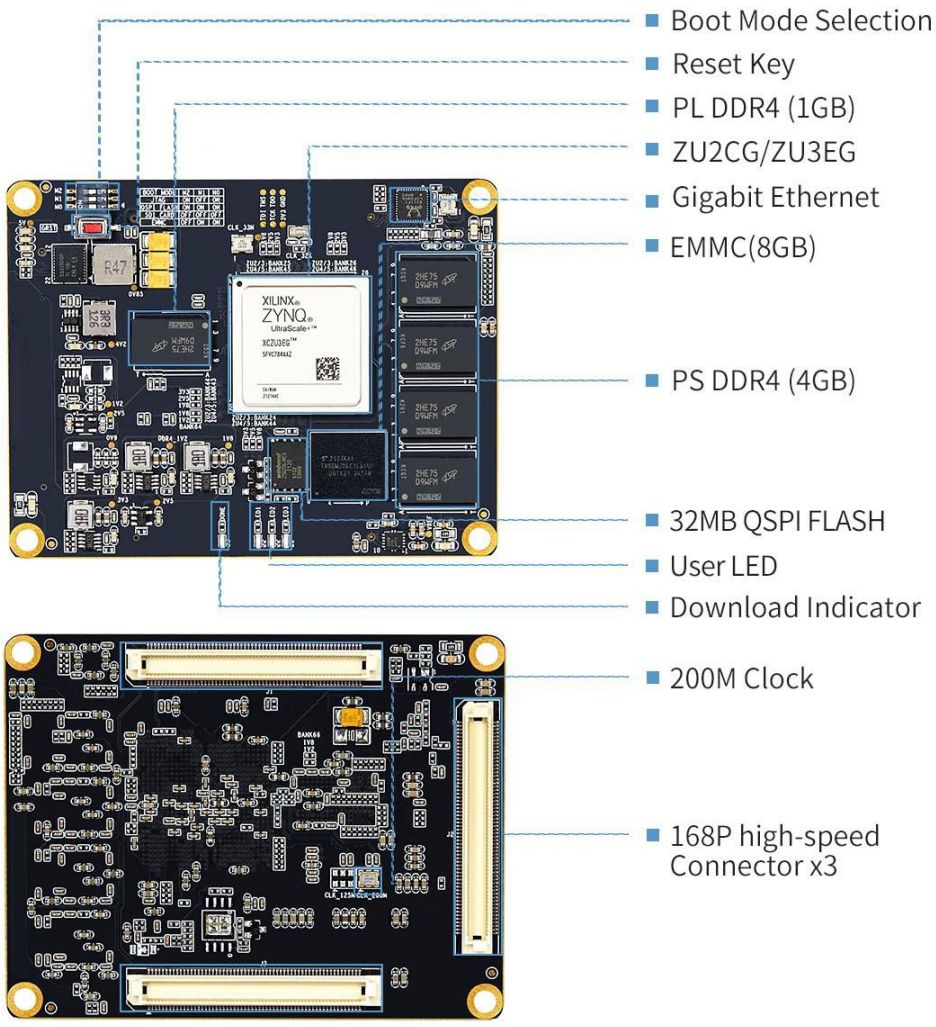
40P expansion port	1, a total of 32 single-ended signals/16 pairs of differential signals
120P expansion port	2, a total of 80 single-ended signals/40 pairs of differential signals
Dimensions	Core Board: 83.8mm x 64.8mm, Carrier Board: 180mm x 122mm
Board to Board Connectors	3 120P 0.6 high speed connectors, Height 3mm
Operating Voltage	12V/3A

Part 3.3: Product Appearance

As shown in the figure below, the position of each main electronic component on the core board is marked, which is convenient for users to view and identify.



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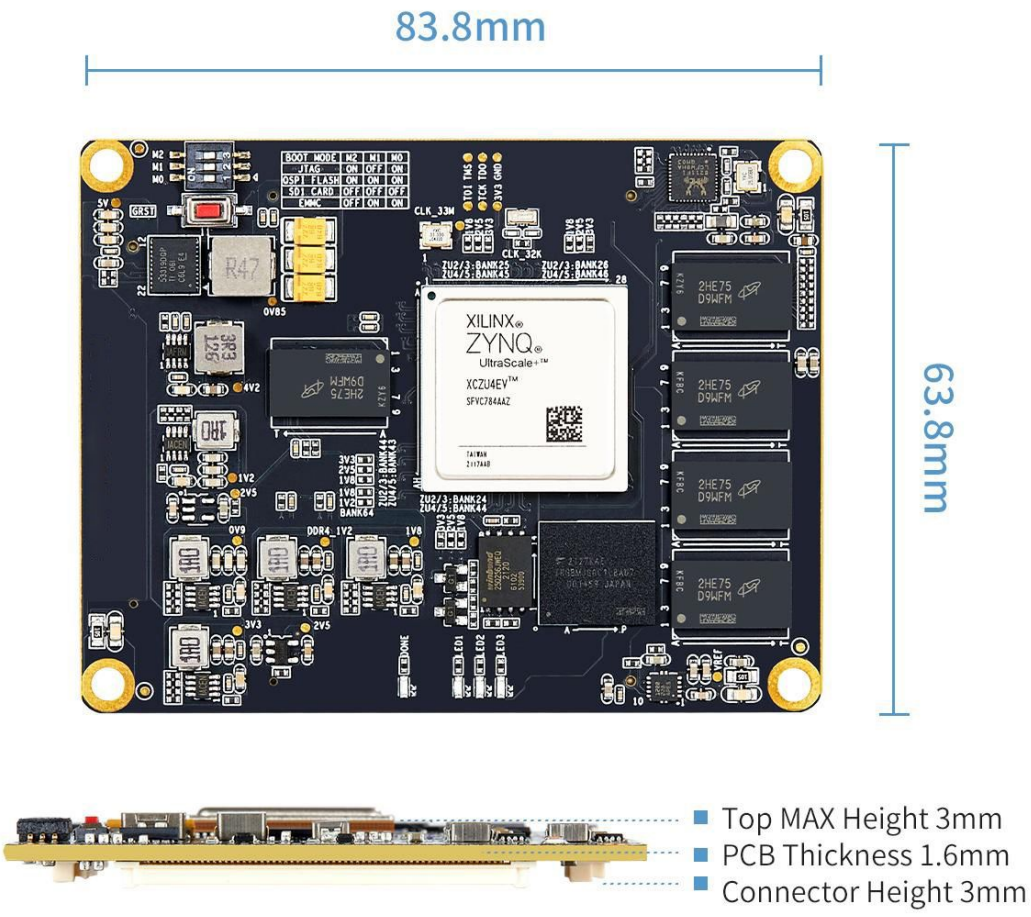
Part 3.4: SOM Form Factors

The Form Factors of the core board is 83.8 x 64.8mm. The core board is connected to the Carrier Board through three 0.6mm/120P gold-plated high-speed connectors on the bottom, with a combined height of 3mm. The following figure shows the dimensions of the core board.



Part 3.5: Power Connection

The power supply voltage of the core board is 5V. There are power input pins on the four corners of the core board. The power pins have been connected inside the module. In the design, you only need to connect the power pin on one corner, and the core board can work. The power connection needs to be connected with copper and enough through holes are made to ensure the power flow capacity. All GND signals on the core board need to be connected to the carrier board, and each GND is connected to the carrier

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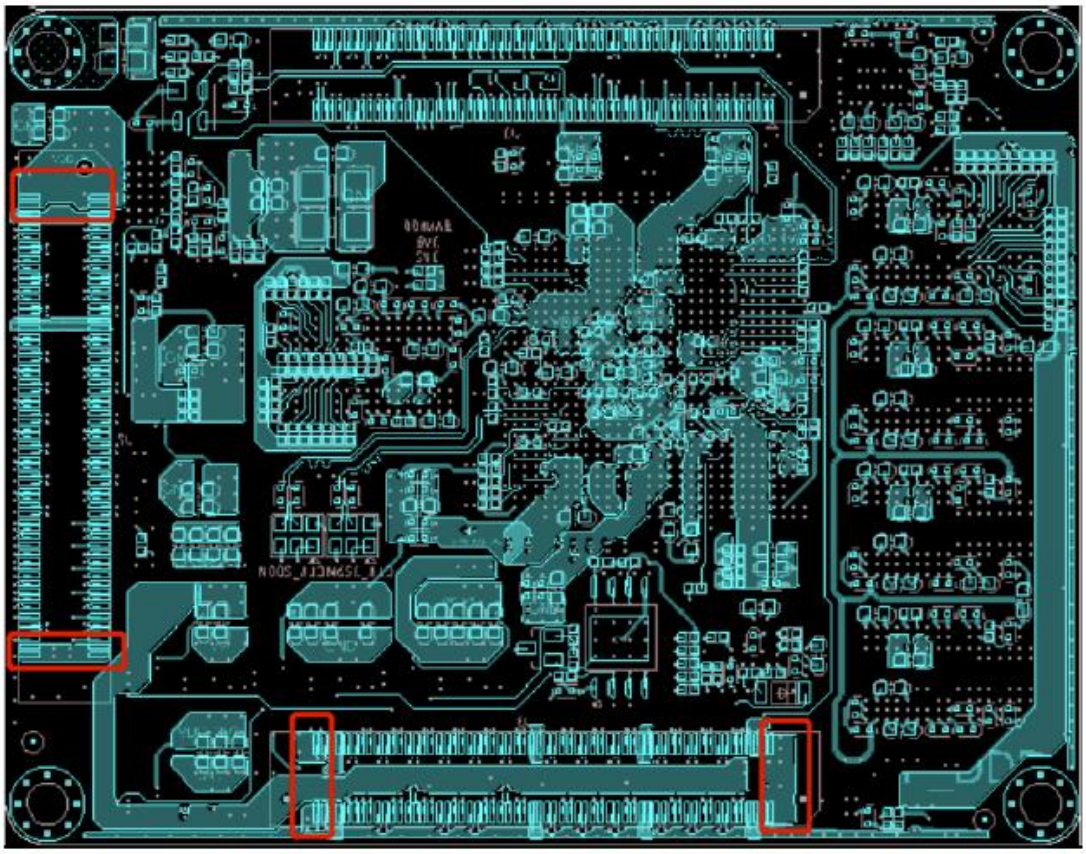
board through two vias. The limit current of the core board power supply is 5A/3A, so the external power supply needs to consider the limit current to ensure the stable operation of the core board.

The output voltage of the power supply to the module needs to be stable. Add a first-level DCDC power conversion to the module power input, from high voltage to 5V, and the DCDC current output capacity can be about 5A. For example, you can refer to the power chip MP2482/MP2225. Two **220uF/25V** capacitors should be placed at the power input of the module to ensure power quality. If you are using tantalum capacitors, it is best to use a 1 ohm 0805 resistor in series with the capacitor to ensure the stability of the tantalum capacitor.



Part 3.6: System Clock

The system clock of the FPGA development board has been prepared on the core board. Three active differential crystal oscillators are placed on the core board, and the PS side is connected to a 33.33M clock; the PL side is

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connected to two clocks. The 200M clock provides the differential clock for the logic side, and the 125M clock provides the differential clock for the GTX interface. As shown in the figure below, the 200M differential clock is connected to the 12P/12N pin of BANK65, the corresponding pin position is L3/L2, and the 125M clock is connected to CLK1 of BANK224, and the corresponding pin is V6/V5. There is no BANK224 for the ZU2/3 platform. , so the 125M clock can only be used on the ZU4/5 platform, but not on the ZU2/3 platform.

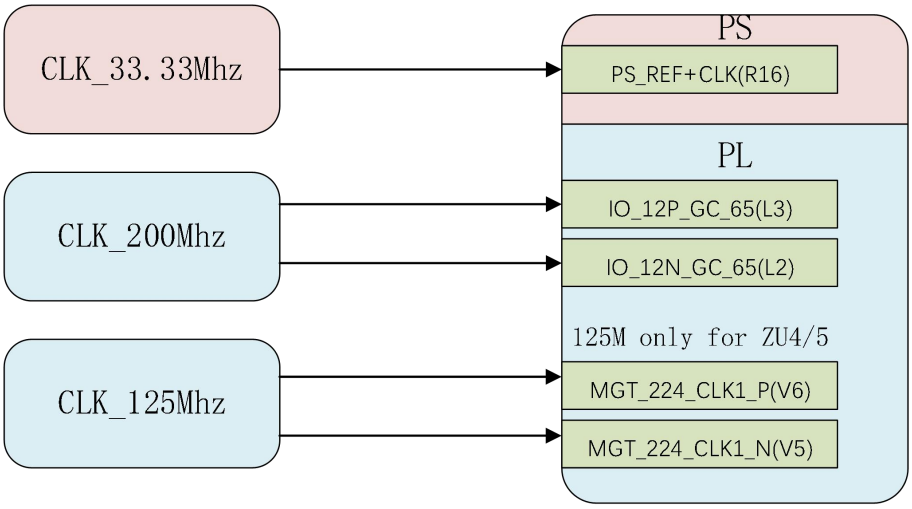

Figure 3-6-1: System Clock Schematic

Part 3.7: Global Reset

The core board provides the “**nGST**” reset key, which is a system reset key and is active at low level. This pin is also drawn to the connector, and the signal name is “**SYS_nRST_I**”, which is convenient for adding a reset key externally or designing a watchdog reset circuit. At the same time, in order to stabilize the system, we added a reset chip MAX811SEUS to the core board. The reset output signal is also led out to the connector, the signal name is SYS_nRST_O. This signal can be used for the reset of other peripherals on the core board. The signal level is 3.3V. The reset pin is a shared reset for PS/PL, which is connected to the PS_POR_500 (D21) pin on the PS side and

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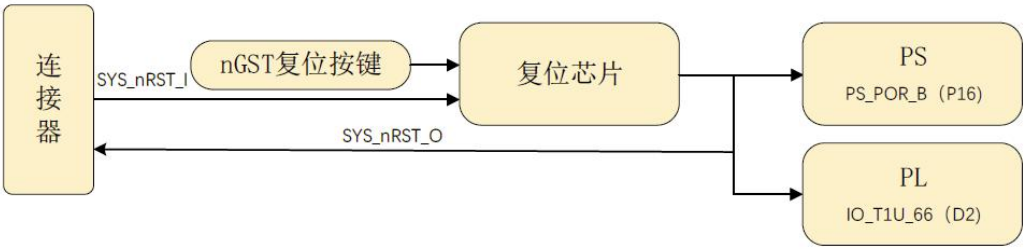
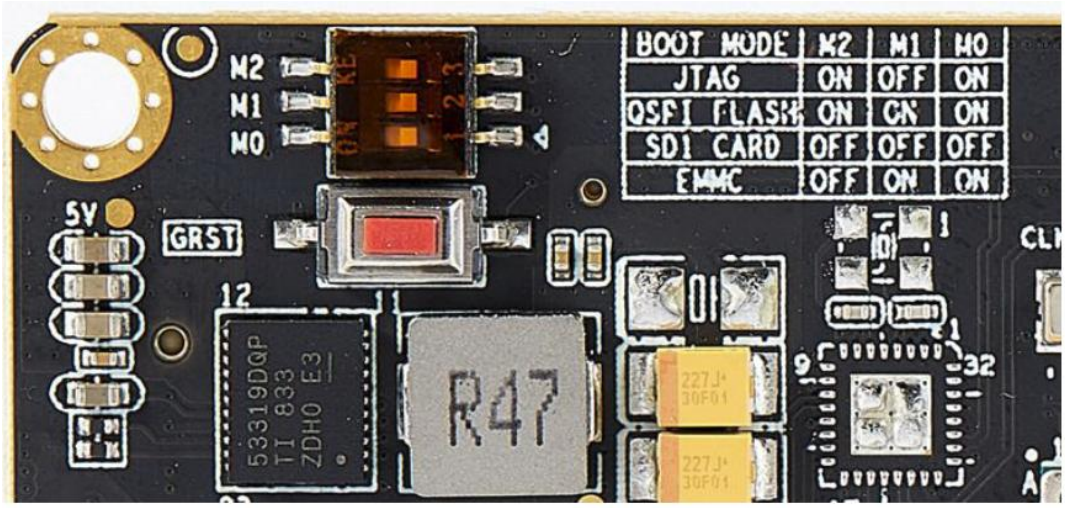
the IO_L3N_34(G9) pin of the BANK44 on the PL side.

If the reset circuit needs to be designed on the carrier board, the following situations need to be considered.

1) The reset circuit board is used internally, only need to add a reset key and a 10uF capacitor parallel port to the ground.
2) The reset circuit needs to be reserved on the structure for external use. It is necessary to add a key to the ground, and at the same time, connect a 10uF capacitor and a TVS anti-static device to the ground in parallel.





Part 3.8: Boot Mode Selection

The core board supports four boot modes, namely JTAG, QSPI Flash, EMMC, and SD card. The first three startup methods are installed on the core board, and users can realize the SD card method by connecting with the carrier board. Four startup methods can be selected through the onboard DIP switch. The following figure has listed the position of each mode DIP switch. Because the main chip generates a large amount of heat, a heat sink needs to be added on the core board, which will block the BOOT MODE selection table.

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BOOT MODE	M2	M1	M0
JTAG	ON	OFF	ON
QSPI FLASH	ON	ON	ON
SD1 CARD	OFF	OFF	OFF
EMMC	OFF	ON	ON

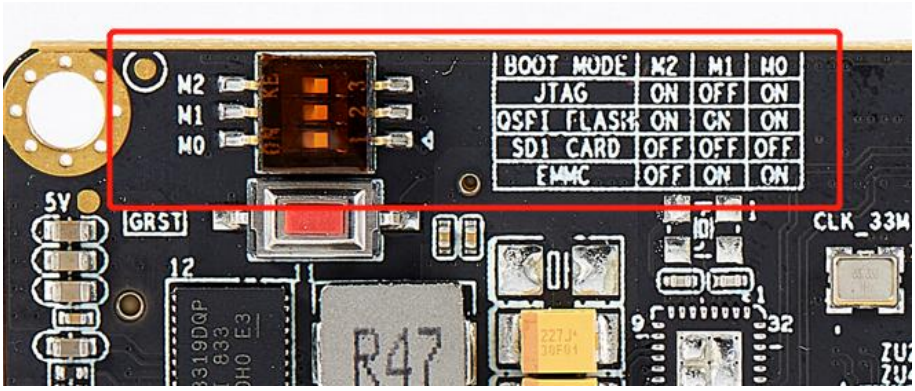

Figure 3-8-1: Boot Mode on Core Board

Part 3.9: Gigabit Ethernet Chip

The Gigabit Ethernet chip KSZ9031 is placed on the core board. The Ethernet chip and the ZYNQ chip are interconnected through the RGMII interface. The corresponding pins are shown in the table below. Ethernet external connection only needs an RJ45 with a transformer to use, the chip address PHY_AD[2:0]=001, the connection schematic diagram can refer to the following figure:

RMGII Signal	Pin Name	Pin Position
GTX_CLK	MIO26_501	L15
TXD0	MIO27_501	J15
TXD1	MIO28_501	K15
TXD2	MIO29_501	G16
TXD3	MIO30_501	F16
TX_EN	MIO31_501	H16
RX_CLK	MIO32_501	J16
RXD0	MIO33_501	L16
RXD1	MIO34_501	L17
RXD2	MIO35_501	H17
RXD3	MIO36_501	K17

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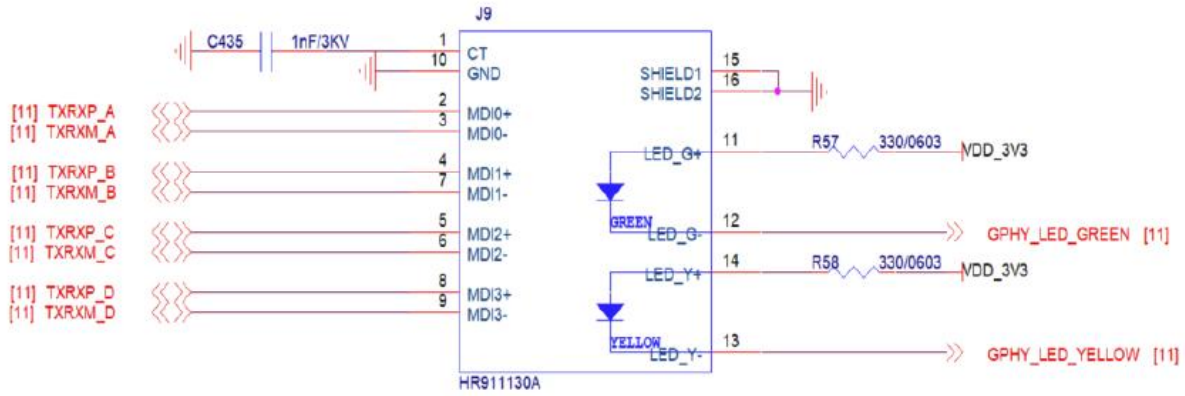
RX_CTL	MIO37_501	J17
MDC	MIO76_502	B20
MDIO	MIO77_502	F20



Part 3.10: EMMC Pin Definition

The onboard EMMC has a capacity of 8GB, and the model will choose an industrial-grade model according to market changes. The pin definitions are as follows.

EMMC Pin	MPSOC Pin Name	Pin Position
EMMC_D0	MIO13	AH18
EMMC_D1	MIO14	AG18
EMMC_D2	MIO15	AE18
EMMC_D3	MIO16	AF18
EMMC_D4	MIO17	AC18
EMMC_D5	MIO18	AC19
EMMC_D6	MIO19	AE19
EMMC_D7	MIO20	AD19
EMMC_CLK	MIO22	AB20
EMMC_CMD	MIO21	AC21
EMMC_nRST	MIO23	AB18

Part 3.11: QSPI FLASH

Two channels of QSPI FLASH are reserved on the core board, QSPI0

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FLASH is attached by default, and QSPI1 FLASH is not attached by default. Users can configure it according to their needs. The onboard QSPI FLASH capacity is 32MB, the model is W25Q256JWEIQ, which is used to store startup files or user files.

QSPI0 FLASH Pin	MPSOC Pin Name	Pin Position
DATA0	MIO4	AH16
DATA1	MIO1	AG16
DATA2	MIO2	AF15
DATA3	MIO3	AH15
QSPI_CS	MIO5	AD16
QSPI_CLK	MIO0	AG15
QSPI0 FLASH Pin	**MPSOC Pin Name**	**Pin Position**
DATA0	MIO8	AF17
DATA1	MIO9	AC16
DATA2	MIO10	AD17
DATA3	MIO11	AE17
QSPI_CS	MIO7	AH17
QSPI_CLK	MIO12	AC17

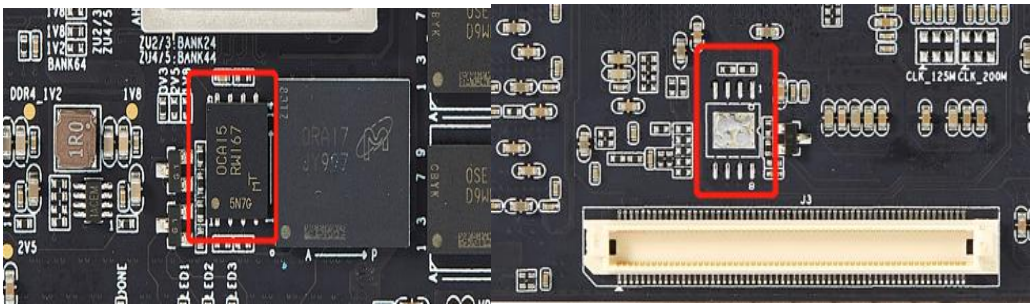

Figure 3-10-1: QSPI Flash on the Core Board

Part 3.12: On-board LED

In order to facilitate debugging, three LEDs are placed on the core board,

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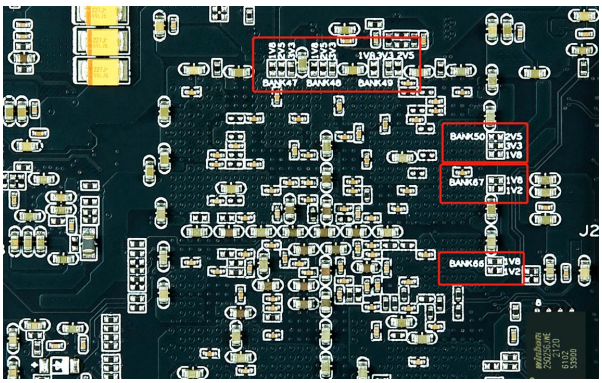
and the LEDs are connected to the PL side. The pin positions of the LEDs are as shown in the table below. When the pin outputs a high level, the LED lights up, and the low level LED goes out.

Number	Pin Name	Pin Position
LED1	IO-T1U-64	AH6
LED2	IO-T2U-64	AB5
LED3	IO-T3U-64	AE4

Part 3.13: BANK Interface Level Selection

The BANK64/66 on the core board are HP BANK, the interface level is configured as 1.2/1.8V, and the voltage can be adjusted by 0 ohm resistance welding through the instructions provided on the single board, and the default level is 1.8V. BANK47/48/49/50 are HD BANK. Also for ZU2/3 and ZU4/5, the naming of HR BANK differs. For ZU2/3 that are BANK24/25/26/44. For ZU4/5, that are B ANK44/45/46/43, and the two BANKs correspond to each other and are pin compatible.BANK level can realize 1.8V/2.5V/3.3V three level conversion, just change the resistor position, the default level is 3.3V.



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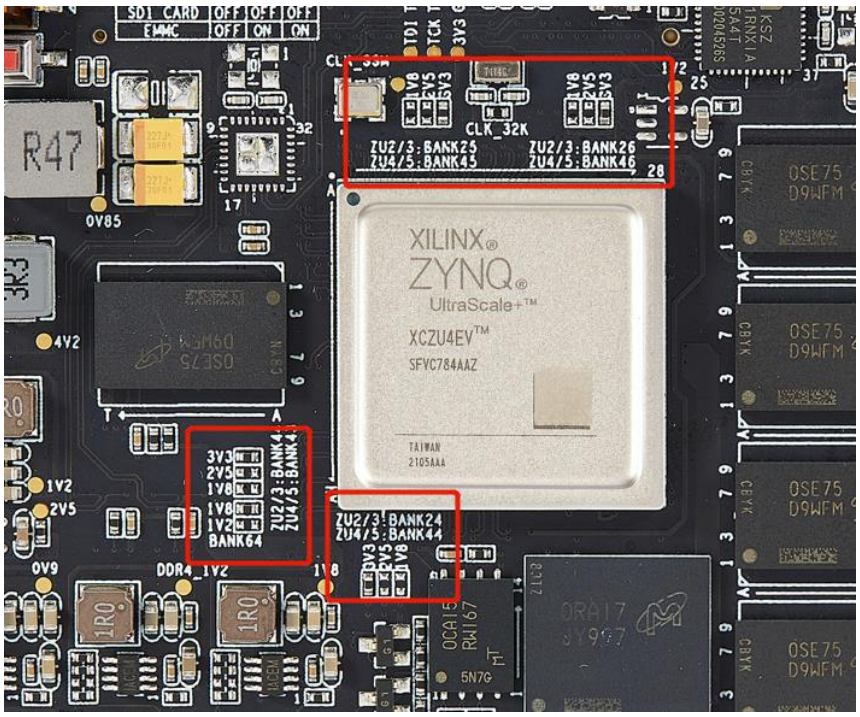

Part 3.14: DDR4 Introduction

DDR4 has been designed on the core board. There are a total of four industrial-grade DDR4 chips on the PS side, with a single capacity of 1GB and a total capacity of 4GB. The model is MT40A512M16LY-062E IT:E , a total of one industrial-grade DDR4 on the PL side. The DDR4 pin on the PS side is a dedicated pin, which can be selected in the software. See the table below for the DDR4 pin assignments on the PL side.

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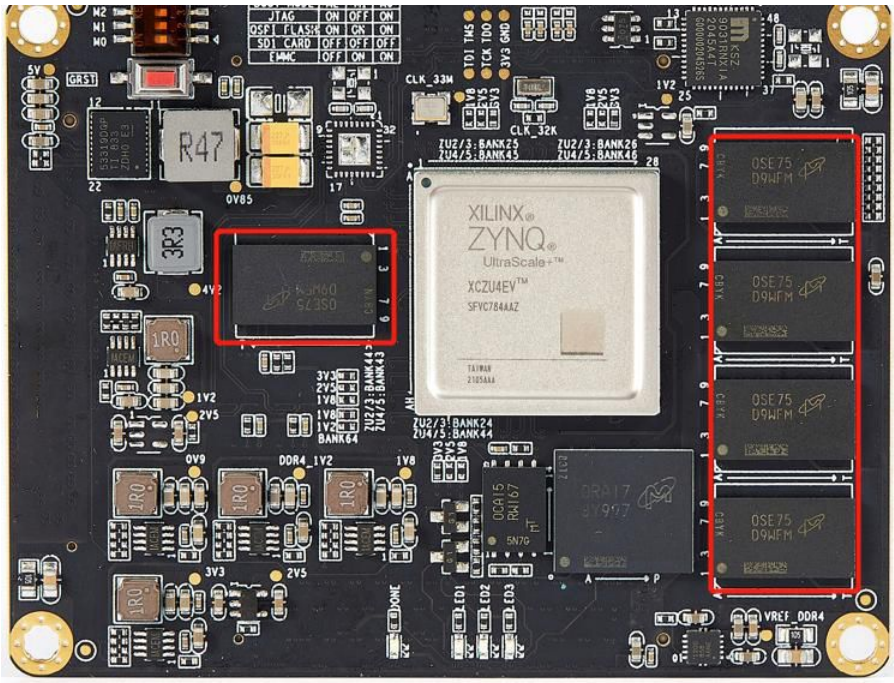

Figure 2-3-7: DDR4 on the Core Board

PL Side DDR4		
DDR4 Pin	**MPSOC Pin Name**	**Pin Position**
DDR4_D0	IO-L20P-65	J6
DDR4_D1	IO-L24P-65	H9
DDR4_D2	IO-L21P-65	J7
DDR4_D3	IO-L23P-65	K9
DDR4_D4	IO-L21N-65	H7
DDR4_D5	IO-L23N-65	J9
DDR4_D6	IO-L20N-65	H6
DDR4_D7	IO-L24N-65	H8
DDR4_DM0	IO-L19P-65	J5
DDR4_DQS_P0	IO-L22P-65	K8
DDR4_DQS_N0	IO-L22N-65	K7
DDR4_D8	IO-L14P-65	M6
DDR4_D9	IO-L17N-65	N8
DDR4_D10	IO-L15N-65	N6
DDR4_D11	IO-L15P-65	N7

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DDR4_D12	IO-L18N-65	L8
DDR4_D13	IO-L17P-65	N9
DDR4_D14	IO-L14N-65	L5
DDR4_D15	IO-L18P-65	M8
DDR4_DM1	IO-L13P-65	L7
DDR4_DQS_P1	IO-L16P-65	P7
DDR4_DQS_N1	IO-L16N-65	P6
DDR4_A0	IO-L8N-65	H1
DDR4_A1	IO-L3P-65	U8
DDR4_A2	IO-L8P-65	J1
DDR4_A3	IO-L3N-65	V8
DDR4_A4	IO-L11P-65	K4
DDR4_A5	IO-L4P-65	R8
DDR4_A6	IO-L9N-65	J2
DDR4_A7	IO-L2P-65	U9
DDR4_A8	IO-L9P-65	K2
DDR4_A9	IO-L1P-65	W8
DDR4_A10	IO-L4N-65	T8
DDR4_A11	IO-L7N-65	K1
DDR4_A12	IO-L6N-65	T6
DDR4_A13	IO-L1N-65	Y8
DDR4_A14	IO-L11N-65	K3
DDR4_A15	IO-L5P-65	R7
DDR4_A16	IO-T2U-65	P9
DDR4_BA0	IO-T1U-65	H2
DDR4_BA1	IO-L5N-65	T7
DDR4_BG0	IO-2N-65	V9
DDR4_CS	IO-L6P-65	R6
DDR4_nACT	IO-L13N-65	L6
DDR4_ODT	IO-L19N-65	J4
DDR4_RESET	IO-L7P-65	L1
DDR4_CLK_P	IO-L10P-65	H4

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DDR4_CLK_N	IO-L10N-65	H3
DDR4_CKE	IO-T3U-65	K5

The PS side is equipped with four industrial-grade DDR4 chips with a single capacity of 1GB and a total capacity of 4GB. The model is MT40A512M16LY-062E. The DDR4 pin assignment can directly call the system assignment. You can also refer to the routines provided by our company.

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Part 4: Carrier Board Introduction

Part 4.1: Operating Voltage

The FPGA development board provides two power supply modes: PCIE interface or 12V/3A power adapter. The power supply options of the two can be selected by the DIP switch S1 on the FPGA development board. When the switch S1 is toggled to the left plug position, use the external adapter to supply power. When the switch S1 is toggled to the right, the PCIE interface is powered.

After the 12V power supply enters the development board, it is converted into 5V/3.3V power supply through the secondary power supply, which is used for the core board and the on-board peripherals. For the detailed circuit, please refer to the schematic diagram of the development board.

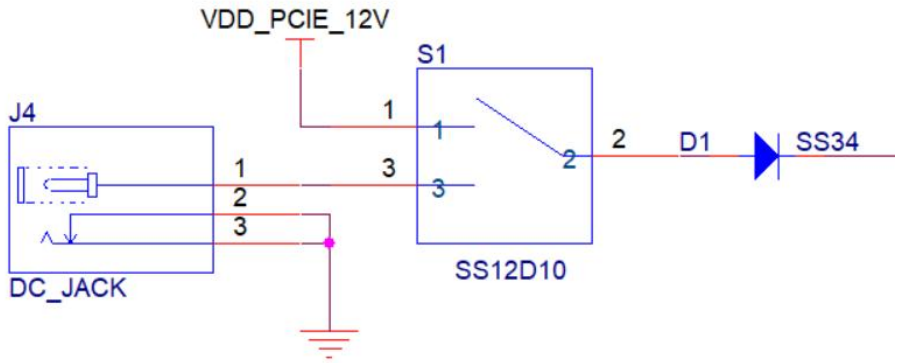

Figure 4-1-1: Power Circuit

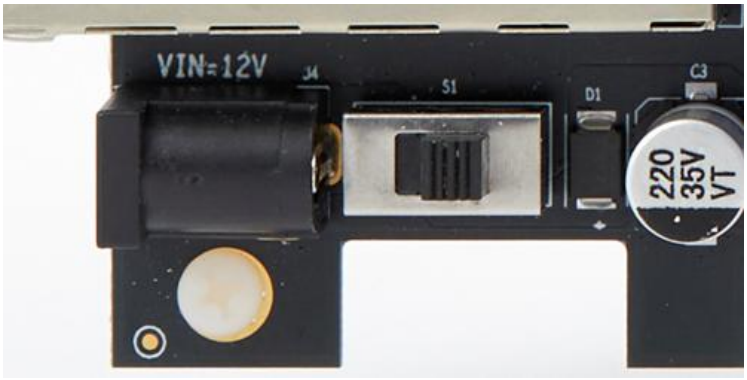

Figure 4-1-2: Power Interface on Carrier Board

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Part 4.2: Reset Circuit

A reset key is reserved on the core board and the carrier board. The two keys are connected together, and the user can choose the key according to the convenience. On the core board circuit, a reset chip is placed after the key, the model is MAX811TEUS. The reset pins are connected to the PS and PL terminals of the MPSOC chip respectively, the PS terminal is connected to BANK0, the corresponding pin is PS_POR_B, the pin location is P16, the PL terminal is connected to BANK65, the corresponding pin is IO_T1U_66, and the pin location is D2. In addition, the reset pin is also connected to the reset pin of EMMC and Gigabit Ethernet for power-on reset.

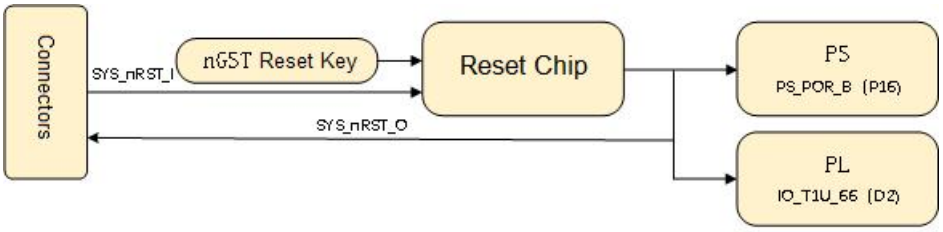

Figure 4-2-1: Reset Circuit Schematic

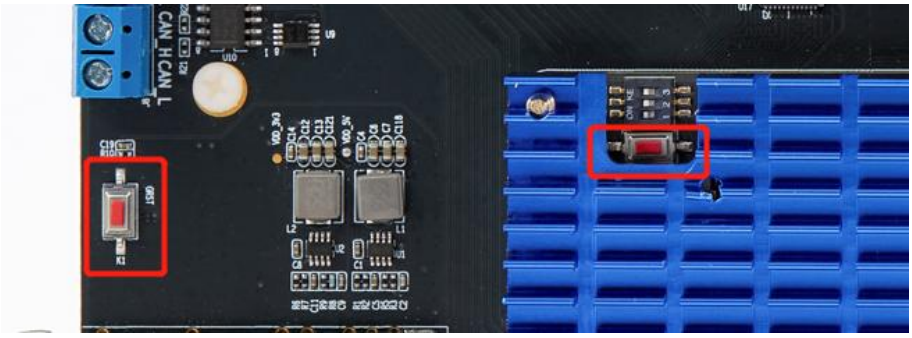

Figure 4-2-2: Reset Circuit on Board

Part 4.3: USB Uart Interface

The development board uses Silicon Labs CP2102GM chip to realize USB to UART, and the USB interface adopts Micro USB. Users only need to use a Micro USB cable to connect to the PC for serial communication. The TX/RX signal of the UART is connected with the BANK501 of the MPSOC, and

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the interface level is 1.8V, so the serial port interface adopts the level conversion to 3.3V and connects with the serial port chip. The following is the signal correspondence table and schematic diagram, the TX/RX direction is defined for the MPSOC side.

UART0 Pin	MPSOC Pin Name	Pin Position
UART0_TX	MIO_43	K19
UART0_RX	MIO_42	L18

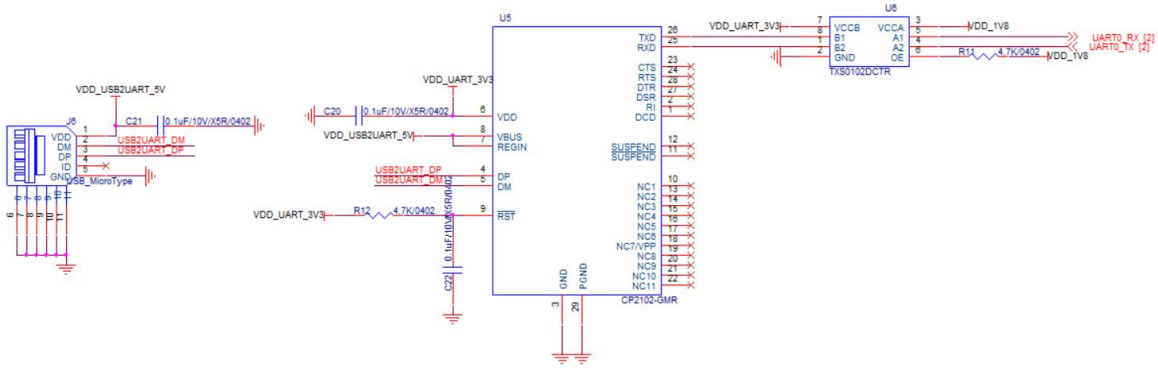

Figure 4-3-1: USB Uart Schematic



Figure 4-3-2: USB Uart on the Carrier Board

Part 4.4: SD Card

A TF card holder is placed on the carrier board, which is convenient for debugging or users to do file storage. The circuit interface level is 1.8V, and the SD card signal is connected to the BANK501 of MPSOC.

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SD Card Pin	MPSOC Pin Name	Pin Location
SD-CLK	MIO51	L21
SD-CMD	MIO50	M19
SD-DATA0	MIO46	L20
SD-DATA1	MIO47	H21
SD-DATA2	MIO48	J21
SD-DATA3	MIO49	M18

The following is the signal correspondence table and schematic, the TX/RX direction is defined by the MPSOC side

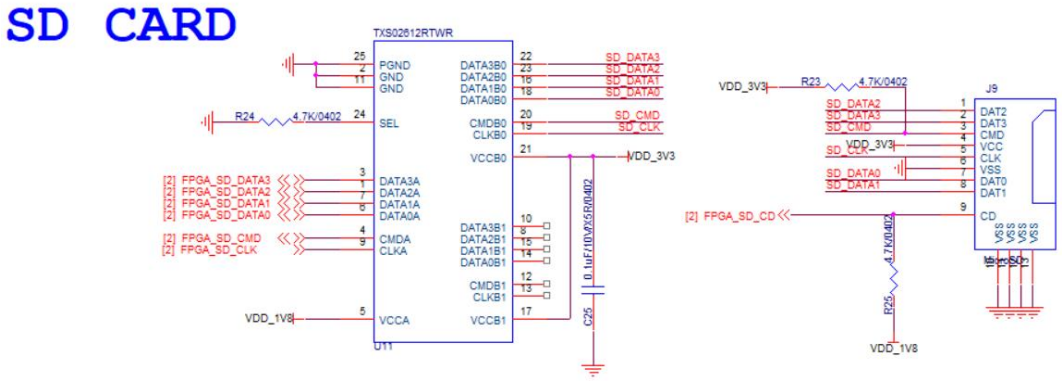

Figure 4-4-1: SD Card Schematic

Part 4.5: RS485 Interface

The FPGA development board uses the SP3485EN chip to realize RS485 communication. The TX/RX signal of RS485 is connected to the BANK501 of the MPSOC, and the interface level is 1.8V, so the interface adopts the level conversion to 3.3V and is connected to the RS485 chip. The following is the signal correspondence table and schematic diagram, the TX/RX direction is defined for the MPSOC side.

RS485 Pin	MPSOC Pin Name	Pin Position
RS485_TX	MIO_40	K18
RS485_RX	MIO_41	J19

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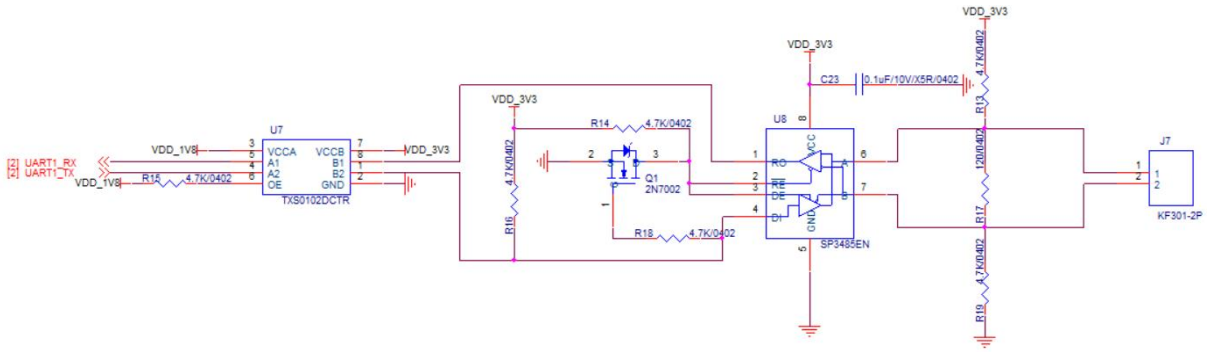

Figure 4-5-1: RS485 Schematic

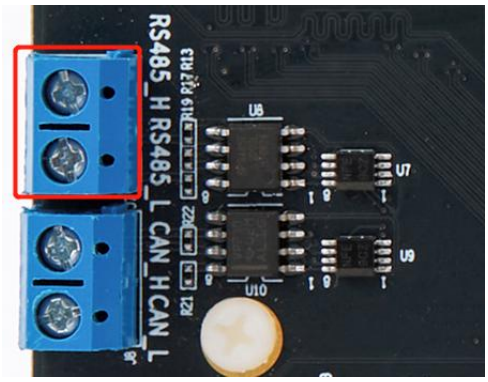

Figure 4-5-2: RS485 on the Carrier Board

Part 4.6: CAN Interface

The FPGA development board uses the SN65HVD230D chip to realize CAN communication. The TX/RX signal of CAN is connected to the BANK501 of the MPSOC, and the interface level is 1.8V, so the serial interface is connected to the CAN chip by level conversion to 3.3V. The following is the signal correspondence table and schematic diagram. The TX/RX direction is defined by the MPSOC side.

CAN Pin	MPSOC Pin Name	Pin Position
CAN_TX	MIO_39	H19
CAN_RX	MIO_38	H18

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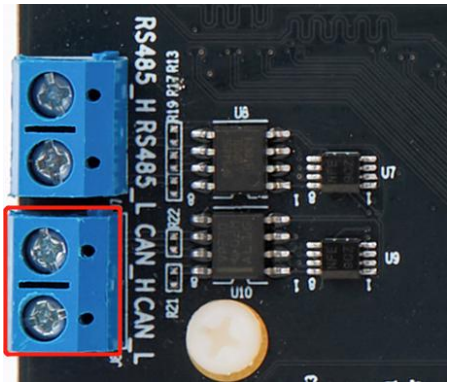

Figure 4-6-1: CAN Interface on the Carrier Board

Part 4.7: E2PROM

A 64Kbit EEPROM chip is placed on the Carrier board, the model is AT24C64D-SSHM-T, which is connected to the BANK44/43 of the FPGA through the IIC bus. The EEPROM read address is 0xA1, and the write address is 0xA0. The following is the pin assignment and schematic diagram of the EEPROM. ZU2/3 corresponds to BANK44, and ZU4/5 corresponds to BANK43.

EEPROM Pin	MPSOC Pin Name	Pin Position
IIC-CLK	IO-6P-HDGC-44/43	AC12
IIC-DATA	IO-6N-HDGC-44/43	AD12

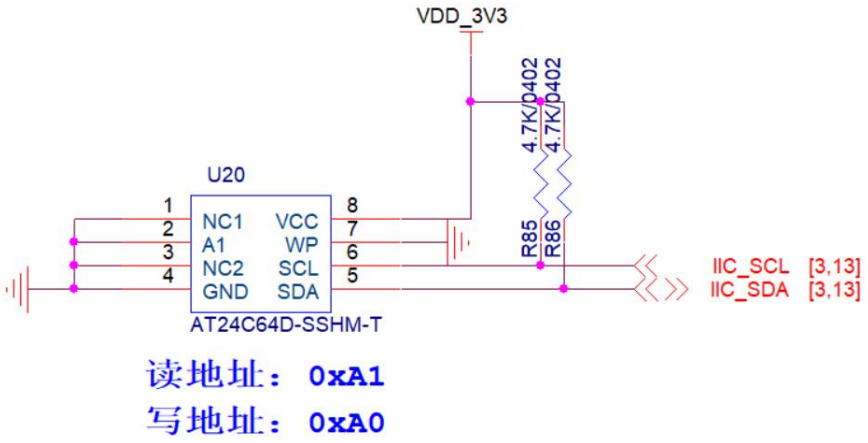

Figure 4-7-1: E2PROM Schematic

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Part 4.8: Mini DP Interface

A Mini DP output interface is placed on the FPGA development board, and the interface signal is connected to the BANK505/BANK26 of the FPGA. For details, please refer to the schematic diagram. ZU2/3 corresponds to BANK26, and ZU4/5 corresponds to BANK46. The following is the pin assignment of Mini DP, the schematic can be viewed under the folder.

Mini DP Pin	MPSOC PIN Name	Pin Position
DP_LINE_P0	MGT_505_TX_P3	B23
DP_LINE_N0	MGT_505_TX_N3	B24
DP_LINE_P1	MGT_505_TX_P2	C25
DP_LINE_N1	MGT_505_TX_N2	C26
DP_HPD	IO_L10N_26_46	H13
DP_AUX_OUT	IO_L1N_26_46	A15
DP_OE	IO_L1P_26_46	B15
DP_AUX_IN	IO_L10P_26_46	H14
DP_CLK_P_27M	MGT_505_CLK_P2	C21
DP_CLK_N_27M	MGT_505_CLK_N2	C22

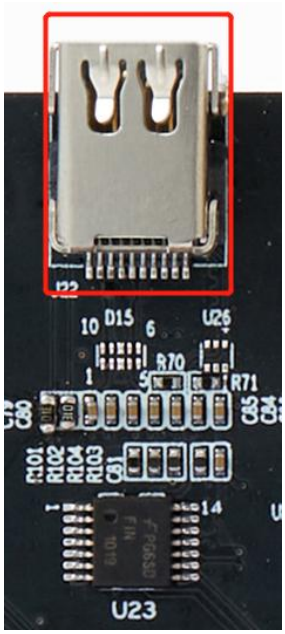

Figure 4-8: Mini DP Interface on the Carrier Board

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Part 4.9: USB 2.0/ USB 3.0

Four USB3.0 main interfaces are placed on the development board, and the main interfaces are compatible with USB2.0/3.0. The interface signal is connected with the BANK501/BANK505 of the FPGA, please refer to the schematic for details. USB2.0 is realized by connecting the PHY chip USB3320C-EZK to MIO. USB3.0 is extended with HUB chip GL3523-OTY30. The following is the pin assignment of USB2.0/USB3.0. The schematics can be viewed under the folder.

USB Pin	MPSOC Pin Name	Pin Position
USBPHY_DATA0	MIO56	C16
USBPHY_DATA1	MIO57	A16
USBPHY_DATA2	MIO54	F17
USBPHY_DATA3	MIO59	E17
USBPHY_DATA4	MIO60	C17
USBPHY_DATA5	MIO61	D17
USBPHY_DATA6	MIO62	A17
USBPHY_DATA7	MIO63	E18
USBPHY_STP	MIO58	F18
USBPHY_NXT	MIO55	B16
USBPHY_DIR	MIO53	D16
USBPHY_CLKOUT	MIO52	G18
USBPHY_RESET	MIO44	J20
GT1_USB3_SSTXP	MGT_505_TX_P1	D23
GT1_USB3_SSTXN	MGT_505_TX_N1	D24
GT1_USB3_SSRXP	MGT_505_RX_P1	D27
GT1_USB3_SSRXN	MGT_505_RX_N1	D28
USB3_CLK_P_26M	MGT_505_CLK_P1	E21
USB3_CLK_N_26M	MGT_505_CLK_N1	E22

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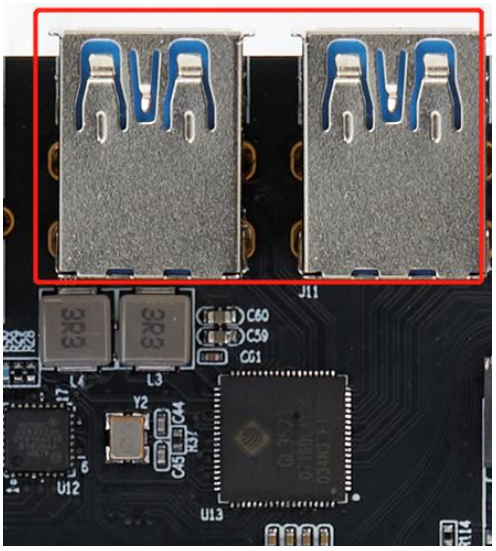

Figure 4-8-1: USB 2.0/ USB 3.0 on the Carrier Board

Part 4.10: Gigabit Ethernet

Two Gigabit Ethernets are designed on the FPGA development board, one for the PS side and one for the PL side, and the PS port network port has been integrated into the core board. The Ethernet chip and the MPSOC are interconnected through the RGMII interface. The corresponding pins are shown in the table below. The network port address of the PS port is PHY_AD[2:0]=001, and the network port address of the PL port is PHY_AD[2:0]=010. The schematics can be viewed under the folder.

PS Side Ethernet		
RMGII Signal	**MPSOC Pin Name**	**Pin Position**
GTX_CLK	MIO26_501	L15
TXD0	MIO27_501	J15
TXD1	MIO28_501	K15
TXD2	MIO29_501	G16
TXD3	MIO30_501	F16
TX_EN	MIO31_501	H16
RX_CLK	MIO32_501	J16
RXD0	MIO33_501	L16
RXD1	MIO34_501	L17
RXD2	MIO35_501	H17

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RXD3	MIO36_501	K17
RX_CTL	MIO37_501	J17
MDC	MIO76_502	B20
MDIO	MIO77_502	F20
PL Side Ethernet		
RMGII Signal	**MPSOC Pin Name**	**Pin Position**
TX_CLK	IO_18P _66	E9
TXD0	IO_10N _66	A4
TXD1	IO_10P _66	B4
TXD2	IO_9N _66	A3
TXD3	IO_9P _66	B3
TX_EN	IO_18N _66	D9
RX_CLK	IO_11P_SRCC_66	D4
RXD0	IO_24N_66	B9
RXD1	IO_22P_66	C8
RXD2	IO_22N_66	B8
RXD3	IO_20P_66	C6
RX_CTL	IO_24P_66	C9
PHY_nRST	IO_20N_66	B6
MDC	IO_6P_66	G5
MDIO	IO_11N_SRCC_66	C4

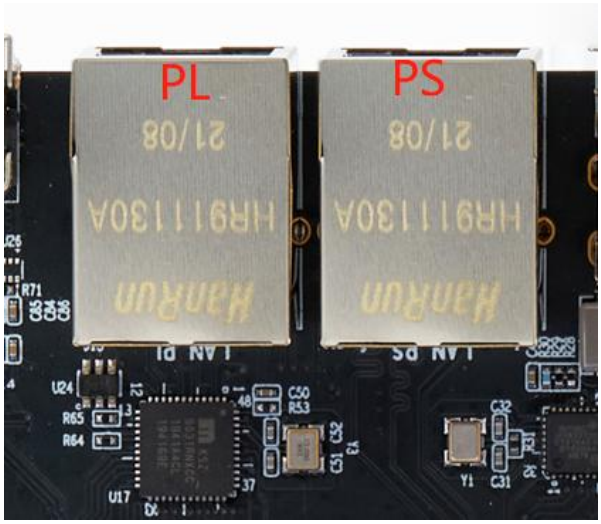

Figure 2-3-18: Gigabit Ethernet on the Carrier Board

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Part 4.11: SFP

Two SFP interfaces are designed on the FPGA carrier board, and the interface signals are connected to BANK25/BANK224 of MPSOC. For details, please refer to the schematic diagram. In addition, ZU2/3 platform does not have BANK224, does not support PCIE, ZU4/5 support. The following is the pin assignment of SFP, the schematic diagram can be viewed under the folder.

SFP1 Pin	MPSOC Pin Name	Pin Position
SFP-TX-P1	MGT-TX-P3-224	N4
SFP-TX-N1	MGT-TX-N3-224	N3
SFP-RX-P1	MGT-RX-P3-224	P2
SFP-RX-N1	MGT-RX-N3-224	P1
SFP1-TX-DISABLE	IO-6P-25/45	F12
SFP1_RxRATE_SEL	IO-6N-25/45	F11

SFP2 Pin	MPSOC Pin Name	Pin Position
SFP-TX-P2	MGT-TX-P2-224	R4
SFP-TX-N2	MGT-TX-N2-224	R3
SFP-RX-P2	MGT-RX-P2-224	T2
SFP-RX-N2	MGT-RX-N2-224	T1
SFP2-TX-DISABLE	IO-4P-25/45	J12
SFP2_RxRATE_SEL	IO-4N-25/45	H12

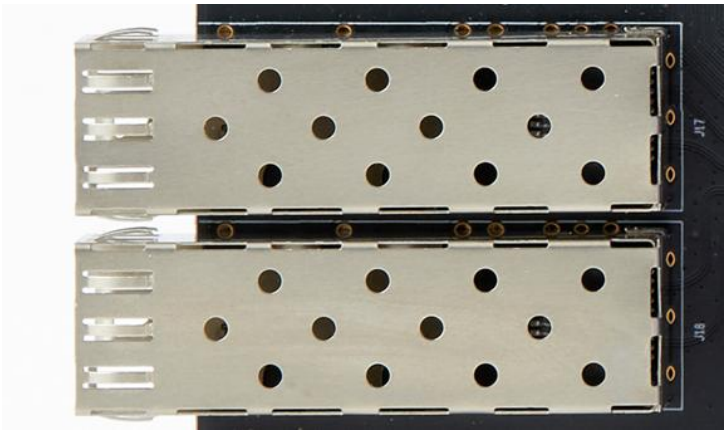

Figure 2-3-19: SFP Interfaces on the Carrier Board

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Part 4.12: PCIE Interface

The PCIE3.0 x2 interface is designed on the FPGA Carrier board, and the interface signal is connected to the BANK44(43)/BANK224 of the FPGA. For details, please refer to the schematic. In addition, ZU2/3 platform does not have BANK224, does not support PCIE, ZU4/5 support.

PCIE Interface	MPSOC Pin Name	Pin Position
PERST_N	IO_5P_GC_44/43	AE12
PCIE_CLK_P	MGT_224_CLK_P0	Y6
PCIE_CLK_N	MGT_224_CLK_N0	Y5
PER0_P	MGT_224_TX_P1	U4
PER0_N	MGT_224_TX_N1	U3
PER1_P	MGT_224_TX_P0	W4
PER1_N	MGT_224_TX_N0	W3
PET0_P	MGT_224_RX_P1	V2
PET0_N	MGT_224_RX_N1	V1
PET1_P	MGT_224_RX_P0	Y2
PET1_N	MGT_224_RX_N0	Y1

Part 4.13: SSD

One SSD (x1 mode) is designed on the PS side of the FPGA development board, the interface type is M.2, and the NVME protocol is used. The pin locations of the SSD interface are shown in the table below.

SSD Interface	MPSOC Pin Name	Pin Position
SSD_nRST	MIO75_502	A19
REFCLK_P_100M	MGT_505_CLK_P0	F23
REFCLK_N_100M	MGT_505_CLK_N0	F24
GT0_SSD_TX_P0	MGT_505_TX_P0	E25
GT0_SSD_TX_N0	MGT_505_TX_N0	E26
GT0_SSD_RX_P0	MGT_505_RX_P0	F27
GT0_SSD_RX_N0	MGT_505_RX_N0	F28

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Figure 2-3-20: SSD on the Carrier Board

Part 4.14: LED

The core board is designed with three LEDs, and the carrier board is designed with five LEDs, totaling 8 LEDs. The LEDs are connected to the PL side and can be assigned to the ARM side through EMIO. The pin positions of the LEDs are as shown in the table below. When the pin outputs a high level, the LED lights up, and when the pin outputs a high level, the LED turns off. The ZU2/3 signal is located at BANK44, and the ZU4/5 signal is located at BANK43.

LED Position	MPSOC Pin Name	Pin Position
LED1 (Core Board)	IO-T1U-64	AH6
LED2 (Core Board)	IO-T2U-64	AB5
LED3 (Core Board)	IO-T3U-64	AE4
LED1 (Carrier Board)	IO-L7N-44/43	AD10
LED2 (Carrier Board)	IO-L7P-44/43	AD11
LED3 (Carrier Board)	IO-L5N-44/43	AF12
LED4 (Carrier Board)	IO-L12P-44/43	AB10
LED5 (Carrier Board)	IO-L12N-44/43	AB9

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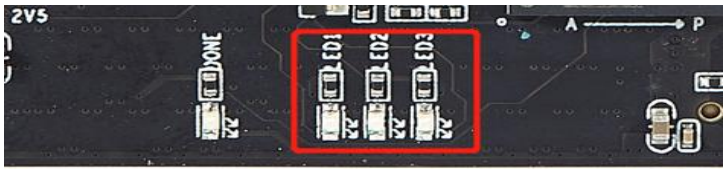

Figure 2-3-21: LEDs on the Core Board



Figure 2-3-22: LEDs on the Carrier Board

Part 4.15: KEYs

The FPGA Carrier is designed with five-way Keys. The key is high level by default, and the key is low level when pressed. The key is connected to the PL side, and can also be assigned to the ARM side through EMIO. The pin location of the key is as follows. The ZU2/3 signal is located at BANK44, and the ZU4/5 signal is located at BANK43.

KEY Number	MPSOC Pin Name	Pin Location
KEY 1	IO-L4P-44/43	AE10
KEY 2	IO-L1N-44/43	AH10
KEY 3	IO-L1P-44/43	AG10
KEY 4	IO-L2N-44/43	AG11
KEY 5	IO-L2P-44/43	AF11

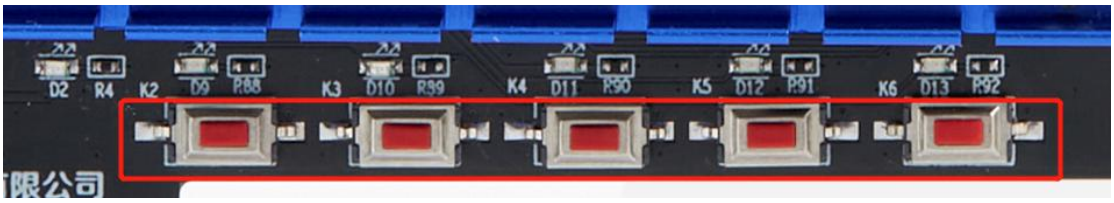

Figure 2-3-23: KYEs on the Carrier Board

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Part 4.16: 40P Expansion Ports

The FPGA Carrier board is equipped with a 40P 2.54mm pitch simple horn socket for extended signal connection, The signal is connected with BANK44(43)/BANK24(44) of FPGA, and the level is 3.3V. The following table indicates the position of the chip where the signal is located. For the detailed connection relationship, please refer to the schematic

Note: ZU2/3 corresponds to BANK44/BANK24, ZU4/5 corresponds to BANK43/44

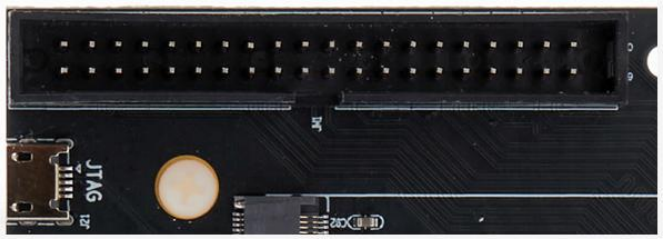

Figure 2-3-24: 40P Expansion Ports on the Carrier Board

JM1 signal sequence	MPSOC Pin Name	Pin Location
5	IO_L10P_44_43	W10
7	IO_L10N_44_43	Y10
9	IO_L8P_HDGC_44_43	AB11
11	IO_L8N_HDGC_44_43	AC11
13	IO_L10P_24_44	Y14
15	IO_L10N_24_44	Y13
17	IO_L7P_HDGC_24_44	AA13
19	IO_L7N_HDGC_24_44	AB13
21	IO_L11P_24_44	W12
23	IO_L11N_24_44	W11
25	IO_L2P_24_44	AG14
27	IO_L2N_24_44	AH14
29	IO_L5P_HDGC_24_44	AD15
31	IO_L5N_HDGC_24_44	AD14
37	IO_L12P_24_44	Y12
39	IO_L12N_24_44	AA12

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6	IO_L9P_44_43	AA11
8	IO_L9N_44_43	AA10
10	IO_L3P_44_43	AH12
12	IO_L3N_44_43	AH11
14	IO_L6P_HDGC_24_44	AC14
16	IO_L6N_HDGC_24_44	AC13
18	IO_L9P_24_44	W14
20	IO_L9N_24_44	W13
22	IO_L8P_HDGC_24_44	AB15
24	IO_L8N_HDGC_24_44	AB14
26	IO_L4P_24_44	AE13
28	IO_L4N_24_44	AF13
30	IO_L1P_24_44	AE15
32	IO_L1N_24_44	AE14
38	IO_L3P_24_44	AG13
40	IO_L3N_24_44	AH13

Part 4.17: 120P Expansion Ports

The FPGA core board has two 120P 0.6mm pitch high-speed connectors for extended signal connections. The level of BANK66 can be adjusted by 1.2/1.8V, the default is 1.8V. The following table indicates the position of the chip where the signal is located. For the detailed connection relationship, please refer to the schematic.

J19 signal sequence	MPSOC Pin Name	Pin Position	J19 signal sequence	MPSOC Pin Name	Pin Position
9	IO_L19	B5	10	IO_L23P_6	A9
11	IO_L19	A5	12	IO_L23N_	A8
15	IO_L21	A7	16	IO_L17P_6	F8
17	IO_L21	A6	18	IO_L17N_	E8
21	IO_L1P	G1	22	IO_L12P_	C3
23	IO_L1N	F1	24	IO_L12N_	C2

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27	IO_L2P	E1	28	IO_L7P_66	C1
29	IO_L2N	D1	30	IO_L7N_6	B1
33	IO_L5P	E4	34	IO_L3P_66	F2
35	IO_L5N	E3	36	IO_L3N_6	E2
39	IO_L4P	G3	40	IO_L16P_6	G8
41	IO_L4N	F3	42	IO_L16N_	F7
45	IO_L13	D7	46	IO_L8P_66	A2
47	IO_L13	D6	48	IO_L8N_6	A1
51	IO_L15	G6	52	IO_L14P_	E5
53	IO_L15	F6	54	IO_L14N_	D5

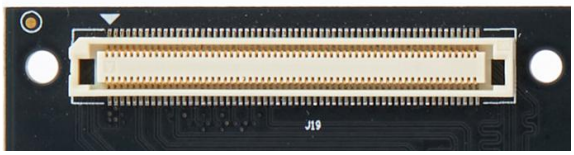

Figure 2-3-25: 40P Expansion Ports on the Carrier Board

J20 signal sequence	MPSOC Pin Name	Pin Position	J20 signal sequence	MPSOC Pin Name	Pin Position
9	IO_L17	AB2	10	IO_L18P_6	AB1
11	IO_L17	AC2	12	IO_L18N_6	AC1
15	IO_L24	AF1	16	IO_L15P_6	AB4
17	IO_L24	AG1	18	IO_L15N_6	AB3
21	IO_L6P	AB6	22	IO_L11P_S	AF7
23	IO_L6N	AC6	24	IO_L11N_S	AF6
27	IO_L10	AG6	28	IO_L5P_64	AB7
29	IO_L10	AG5	30	IO_L5N_64	AC7
33	IO_L9P	AH8	34	IO_L1P_64	AC9
35	IO_L9N	AH7	36	IO_L1N_64	AD9
39	IO_L21	AE3	40	IO_L3P_64	AB8
41	IO_L21	AF3	42	IO_L3N_64	AC8
45	IO_L19	AG4	46	IO_L23P_6	AH2
47	IO_L19	AH4	48	IO_L23N_6	AH1
51	IO_L8P	AF8	52	IO_L16P_6	AD2
53	IO_L8N	AG8	54	IO_L16N_6	AD1
57	IO_L14	AC4	58	IO_L22P_6	AE2

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59	IO_L14	AC3	60	IO_L22N_6	AF2
63	IO_L7P	AG9	64	IO_L13P_	AD5
65	IO_L7N	AH9	66	IO_L13N_	AD4
69	IO_L12	AE5	70	IO_L4P_64	AD7
71	IO_L12	AF5	72	IO_L4N_64	AE7
75	IO_L2P	AE9	76	IO_L20P_6	AG3
77	IO_L2N	AE8	78	IO_L20N_6	AH3

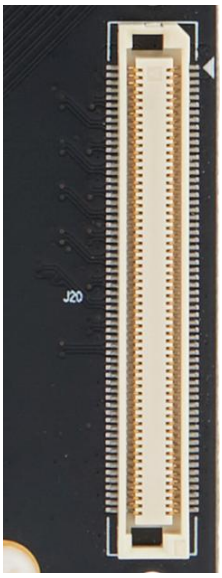

Figure 2-3-26: 40P Expansion Ports on the Carrier Board

Part 4.18: Onboard JTAG Downloader

The FPGA Carrier board is equipped with a USB to JTAG downloader. install the Vivado software, connect the USB port corresponding to the JTAG port, and check whether the MPSOC is recognized.

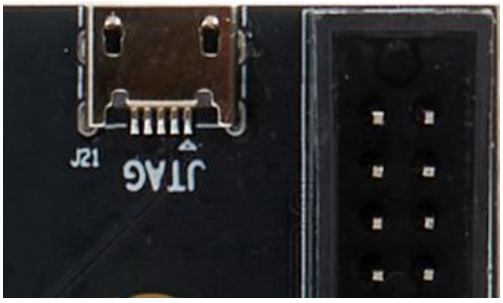

Figure 2-3-27: JTAG on the Carrier Board

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