AMD Virtex UltraScale+

CRVU9PB/ CRVU13PB

User Manual



Version Records:

Data	Version	Description
2025.01.01	V1.0	initial version

This tutorial will continue to revise, optimize and increase based on the actual Experience, that is to provide you with more and better Demos.

If you find some errors or any suggestion, contact with us.

Content

Version Records: 2
Par1: AMD Virtex UltraScale+ FPGA 4
Part 2: Product Overview 6
Part 2.1: Board Introduction 6
Part 2.2: Product Function Block Diagram 7
Part 2.3: Form Factors 7
Part 3: SOM FPGA Core Board 9
Part 3.1: SOM Introduction 9
Part 3.2: SOM Form Factors and Specification 10
Part 3.3: Power Connection 11
Part 3.4: SOM Clock 11
Part 3.5: SOM Reset Key 13
Part 3.6: Boot Mode Selection 13
Part 3.7: BANK Interface Level Selection 13
Part 3.8: Dual Group of DDR4 (8GB+8GB) 14
Part 3.9: SOM Signals with Equal Length 19
Part 3.10: Core Board Package Library 20
Part 3.11: Core Board Connectors 20
Part 4: Carrier Board Overview 21
Part 4.1: Power Supply 21
Part 4.2: System Clock 21
Part 4.3: System Reset 21
Part 4.4: USB to UART 22
Part 4.5: SD Card Slot Interface 22
Part 4.6: E2PROM 23
Part 4.7: Gigabit Ethernet 23
Part 4.8: QSFP28 Interface 24
Part 4.9: SMA Interface 26
Part 4.10: SATA Interface 26
Part 4.11: LED 27
Part 4.12: KEY 27
Part 4.13: FMC Expansion Port 28
Part 4.14: PCIE 3.0 Interface 36
Part 4.15: USB to JTAG Programmer 37

Par1: AMD Virtex UltraScale+ FPGA

Based on the UltraScale™ architecture, the latest Virtex® UltraScale+™ devices provide the highest performance and bandwidth in a 16nm FinFET node.

Virtex UltraScale+ FPGAs are capable of pushing the system performance-per-watt envelope, enabling breakthrough speeds with high utilization. High system performance and multiple power reduction innovations make Virtex UltraScale+ FPGAs the logical choice for compute intensive applications.

The foundation of Virtex UltraScale+ FPGAs has been extended by leveraging Xilinx's modular chip architectures. Xilinx also provides scalability and package migration for the lowest risk and the highest value programmable technology to maximize your return on investment.

HIGHLIGHTS

✓ **Programmable System Integration**

- Up to 9M system logic cells
- Up to 16GB inpackage HBM DRAM
- Up to 500Mb of total on-chip integrated memory
- Integrated 100G Ethernet MAC with KR4 RS-FEC and 150G Interlaken cores
- Integrated blocks for PCI Express® Gen3 x16 and Gen4 x8

✓ **Increased System Performance**

- Up to 38 TOPs (22 TeraMACs) of DSP compute performance
- Up to 128 transceivers operating at 32.75Gb/s or 58Gb/s
- 2,666Mb/s DDR4 in the mid speed grade

✓ **Total Power Reduction**

- Industry's most energy-efficient machine learning inference
- Voltage scaling options to tune for performance and power

✓ **Accelerated Design Productivity**

- Seamless footprint migration from 20nm planar to 16nm FinFET+
- Co-optimized with Vivado® Design Suite for rapid design closure

Virtex UltraScale+ device resources are listed in the table below. We chose two chips, VU9P and VU13P, to design the SOM core board and FPGA development board.

		Foundation						
	Device Name	VU3P	VU5P	VU7P	VU9P	VU11P	VU13P	VU19P
	System Logic Cells (K)	862	1,314	1,724	2,586	2,835	3,780	8,938
	CLB Flip-Flops (K)	788	1,201	1,576	2,364	2,592	3,456	8,172
	CLB LUTs (K)	394	601	788	1,182	1,296	1,728	4,086
	Max. Dist. RAM (Mb)	12.0	18.3	24.1	36.1	36.2	48.3	58.4
	Total Block RAM (Mb)	25.3	36.0	50.6	75.9	70.9	94.5	75.9
	UltraRAM (Mb)	90.0	132.2	180.0	270.0	270.0	360.0	90.0
	DSP Slices	2,280	3,474	4,560	6,840	9,216	12,288	3,840
	Peak INT8 DSP (TOP/s)	7.1	10.8	14.2	21.3	28.7	38.3	10.4
	PCIe® Gen3 x16	2	4	4	6	3	4	0
	PCIe Gen3 x16/Gen4 x8 / CCIX[1]	–	–	–	–	–	–	8
	150G Interlaken	3	4	6	9	6	8	0
	100G Ethernet w/ KR4 RS-FEC	3	4	6	9	9	12	0
	Max. Single-Ended HP I/Os	520	832	832	832	624	832	1,976
	Max. Single-Ended HD I/Os	0	0	0	0	0	0	96
	GTY 32.75Gb/s Transceivers	40	80	80	120	96	128	80
	GTM 58Gb/s PAM4 Transceivers	–	–	–	–	–	–	–
	100G / 50G KP4 FEC	–	–	–	–	–	–	–
	Extended[2]	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2 -2L -3	-1 -2
	Industrial	-1 -2	-1 -2	-1 -2	-1 -2	-1 -2	-1 -2	–
	Footprint[3,4,5] Dim. (mm)				HP I/O, GTY			HP I/O, HD I/O, GTY
Footprint compatible with 20nm UltraScale Devices with same footprint identifier	A1365[4] 35x35							
	C1517 40x40	520, 40						
	J1760 42.5x42.5							
	F1924[6] 45x45					624, 64		
	A2104 47.5x47.5		832, 52	832, 52	832, 52			
	A2104 52.5x52.5[7]						832, 52	
	B2104 47.5x47.5		702, 76	702, 76	702, 76	572, 76		
	B2104 52.5x52.5[7]						702, 76	
	C2104 47.5x47.5		416, 80	416, 80	416, 104	416, 96		
	C2104 52.5x52.5[7]						416, 104	
	D2104 47.5x47.5				676, 76	572, 76		
	D2104 52.5x52.5[7]						676, 76	
	H2104 47.5x47.5							
	A2577 52.5x52.5				448, 120	448, 96	448, 128	
	A3824 65x65							1976, 96,48
	B3824 65x65							1664, 96, 80

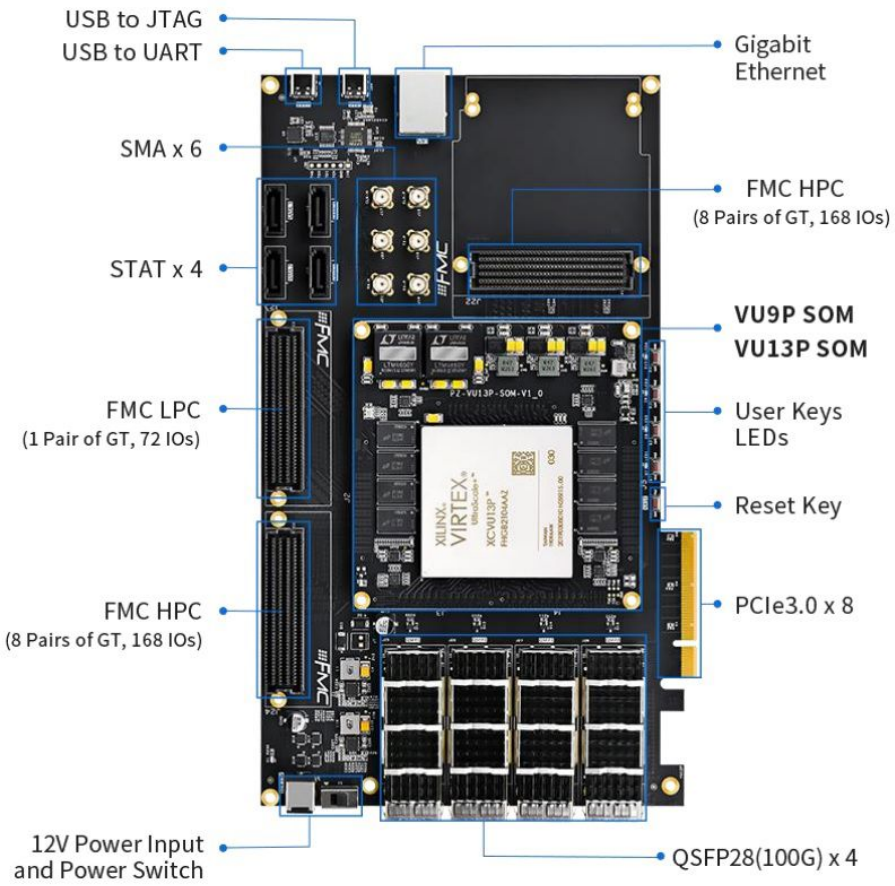
Part 2: Product Overview

Part 2.1: Board Introduction

The Virtex UltraScale+ series of FPGA development boards offerstwo compatible version, respectively, using the XILINX company's XCVU9P-2FLGB2104I and XCVU13P-2FHGB2104I as the main controller.

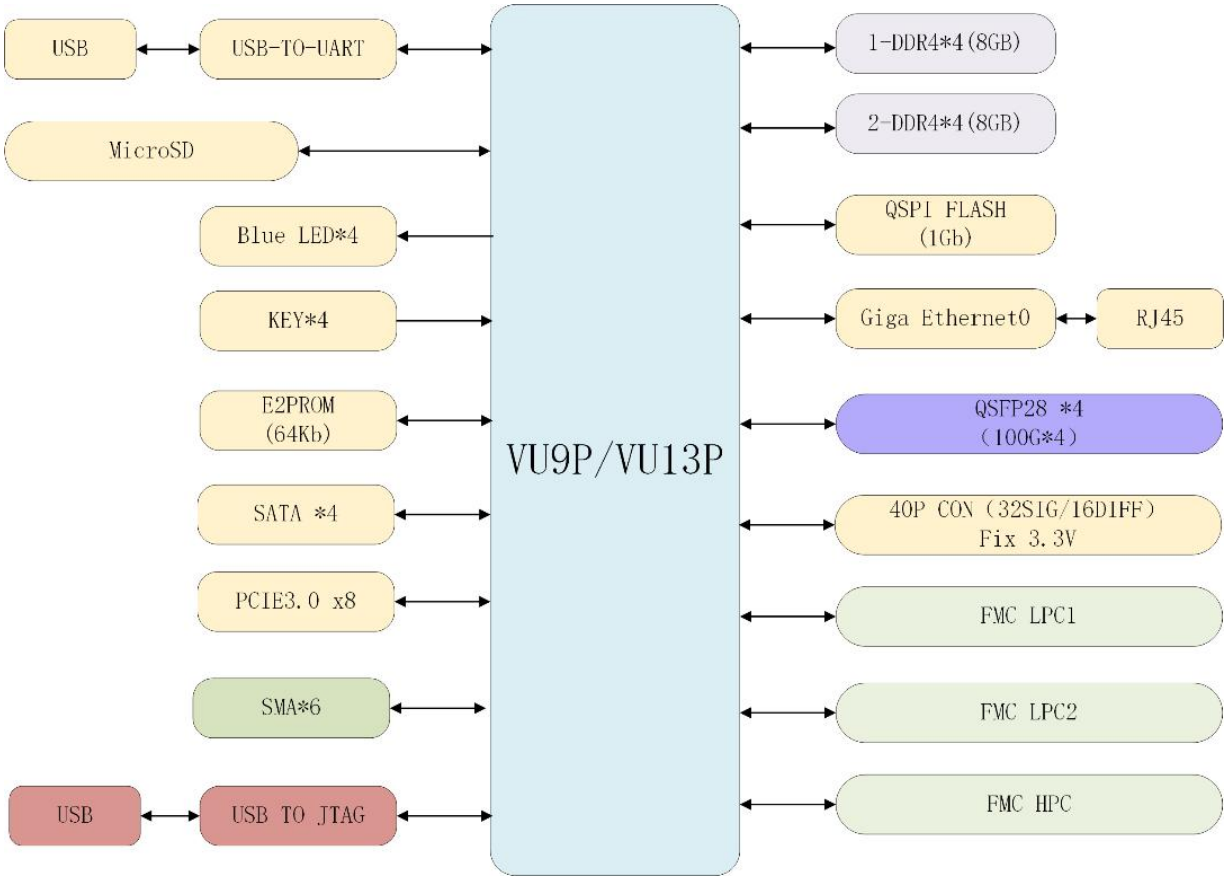
The Virtex UltraScale+ series FPGA development board adopts the mode of “Core board + Carrier board”. The core board is snapped to the carrier board with five 0.635mm pitch 240P high-speed connectors for more flexible use. It can be used for learning or for project development.

In addition, the FPGA development board integrates a wealth of peripheral resources, provides detailed development Demos, and accelerates user learning or project advancement. In addition, the development board also integrates a JTAG debugger, so that a USB cable and a 12V power cable can make the development board work and be more convenient to use.



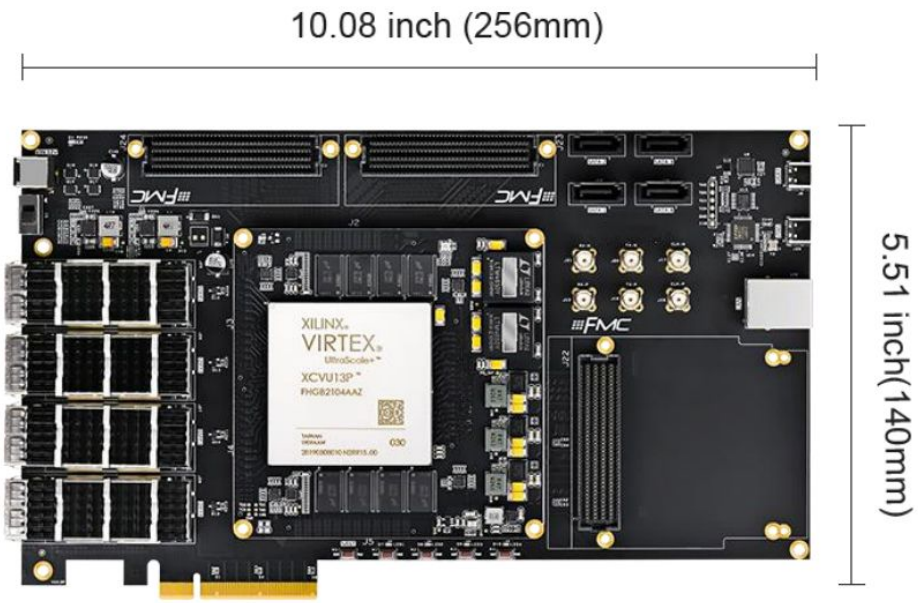
Part 2.2: Product Function Block Diagram

In this section, we will show the configuration details of the product in detail through the product block diagram and product specifications, as shown below.

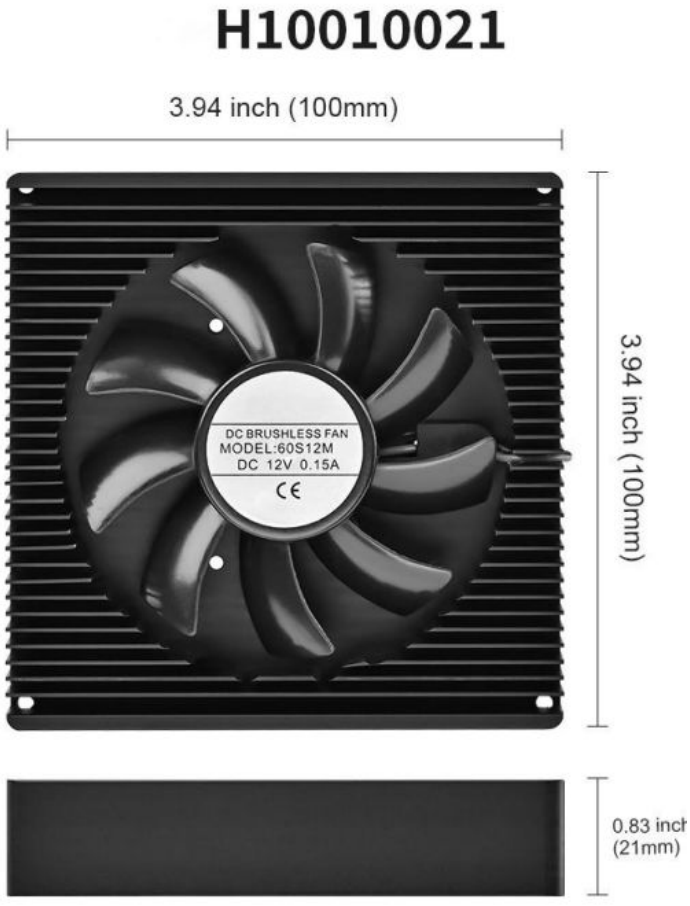


Part 2.3: Form Factors

The form factor of the CRVU13PB/CRVU9PB is 10.08 inch x 5.51 inch (256mm x 140mm), the four corners of the veneer are placed in a fixed hole for the installation of support columns or fixed veneer, the hole diameter of 3.5mm.



The heat dissipation is made up of customized fans, heat sinks. and acrylic protective plate, for the convenience of display, and not installed on the FPGA development board. The form factors of the heat dissipation as below:

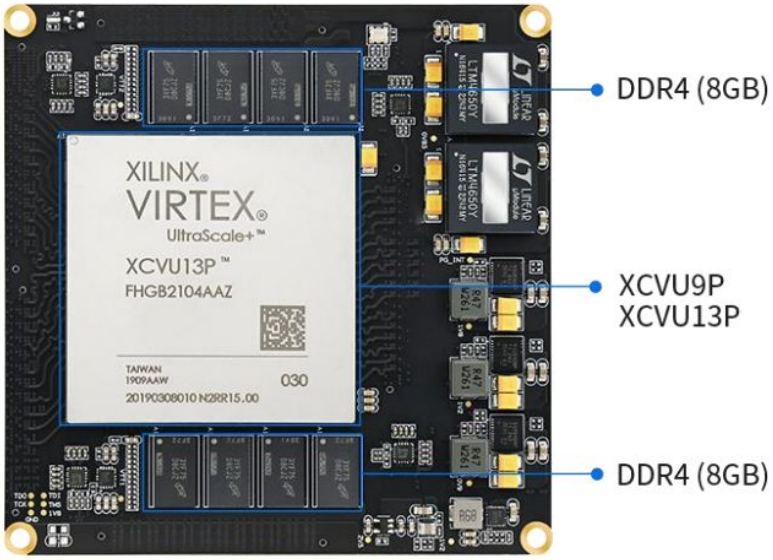


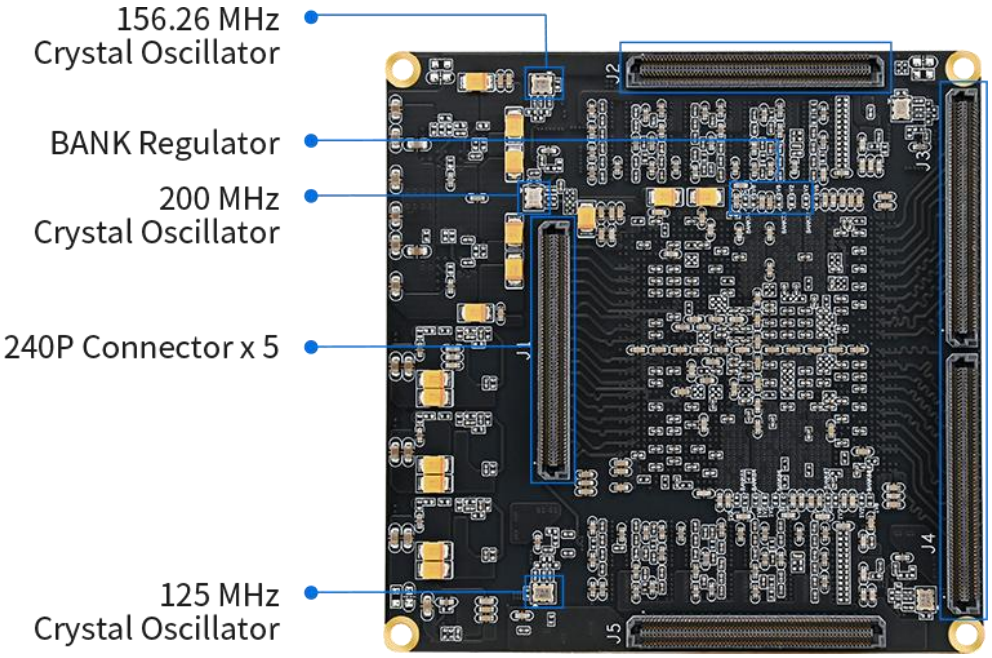
Part 3: SOM FPGA Core Board

Part 3.1: SOM Introduction

The FPGA development board adopts the SOM core board snapping to the carrier board, The SOM core board provides two models, CRVU9PC and CRVU13PC, which are fully compatible.

In this section, we will introduce the two SOM core boards in details.





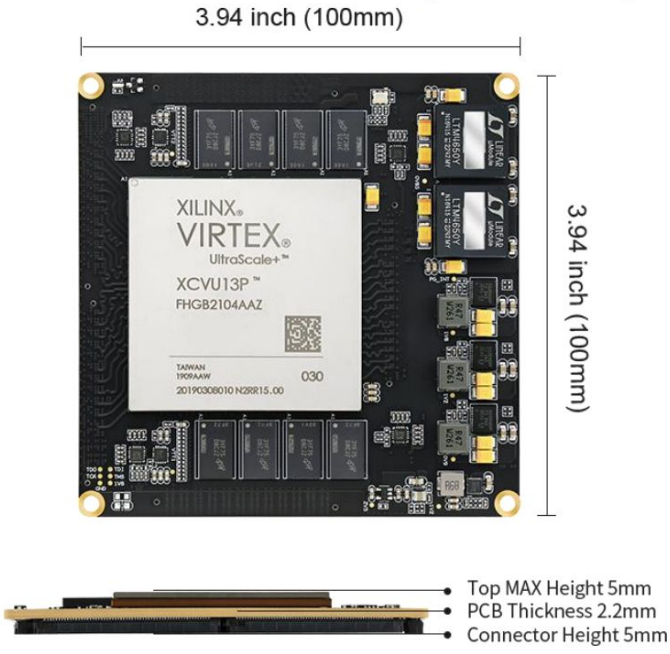
Part 3.2: SOM Form Factors and Specification

The compare table below list all on-board resource, detailed comparison of the two core board differences: the main control chip is different, the same peripheral resources.

Core Board Main Parameters

FPGA Dev. Board	VU9P	VU13P
FPGA Chip	XCVU9P-2FLGB2104I	XCVU13P-2FHGB2104I
Speed Grade	2	
Chip Level	Industrial Grade (-40°C~+85°C)	
Logic Cells	2586k	3780k
Lookup Tables (LUTs)	1182k	1728k
Flip-Flops	2364k	3456k
DSP Slices	6840	12288
BLOCK RAM	75.9Mb	94.5Mb
DDR4	Dual Group of DDR4 (8GB+8GB)	
Start-up Mode	JTAG/ BPI/ SPI, JTAG Startup by default	
Number of IO	360 single-ended/180 differential pairs (1.2/1.8V adjustable, default 1.8V)	
Number of GTY	76 Pairs of TX/RX	
Crystal Oscillator	200MHz Differential Crystal for FPGA 125MHz and 156.25MHz Differential Crystal for the GT Transceiver Reference Clock	
Core Board Form Factors	3.94 inch x 3.94 inch (100mm x 100mm)	

The core board form factors is 3.94 inch x 3.94 inch (100mm x 100mm)

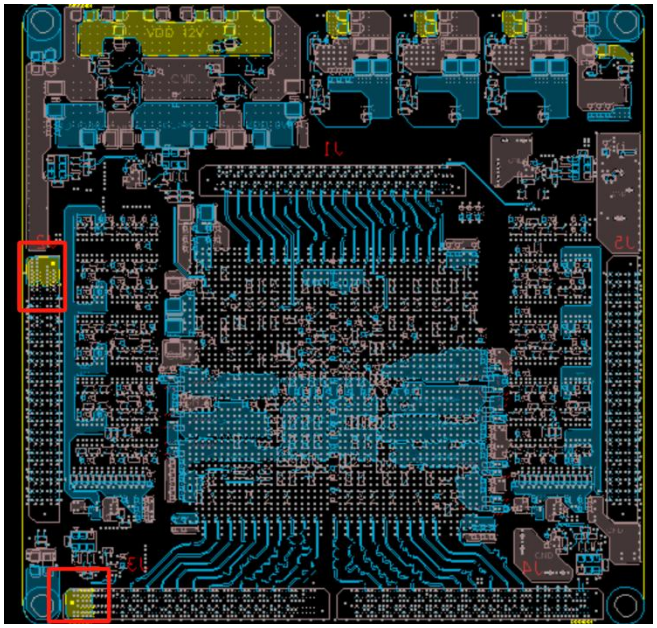


Part 3.3: Power Connection

The SOM core board power supply voltage is 12V, in the two corners of the core board are reserved with power input pins, and the power pins have been connected inside the module, taking into account the chip consumption current is large, so the power supply of the two corners need to be connected to an external power supply, to ensure that the power supply current is sufficient. The power connection needs to be connected with copper and enough holes are made to ensure the power flow ability. All GND signals on the module need to be connected to the base plate, and each GND is connected to the carrier board through two through-holes to ensure through-flow capability.

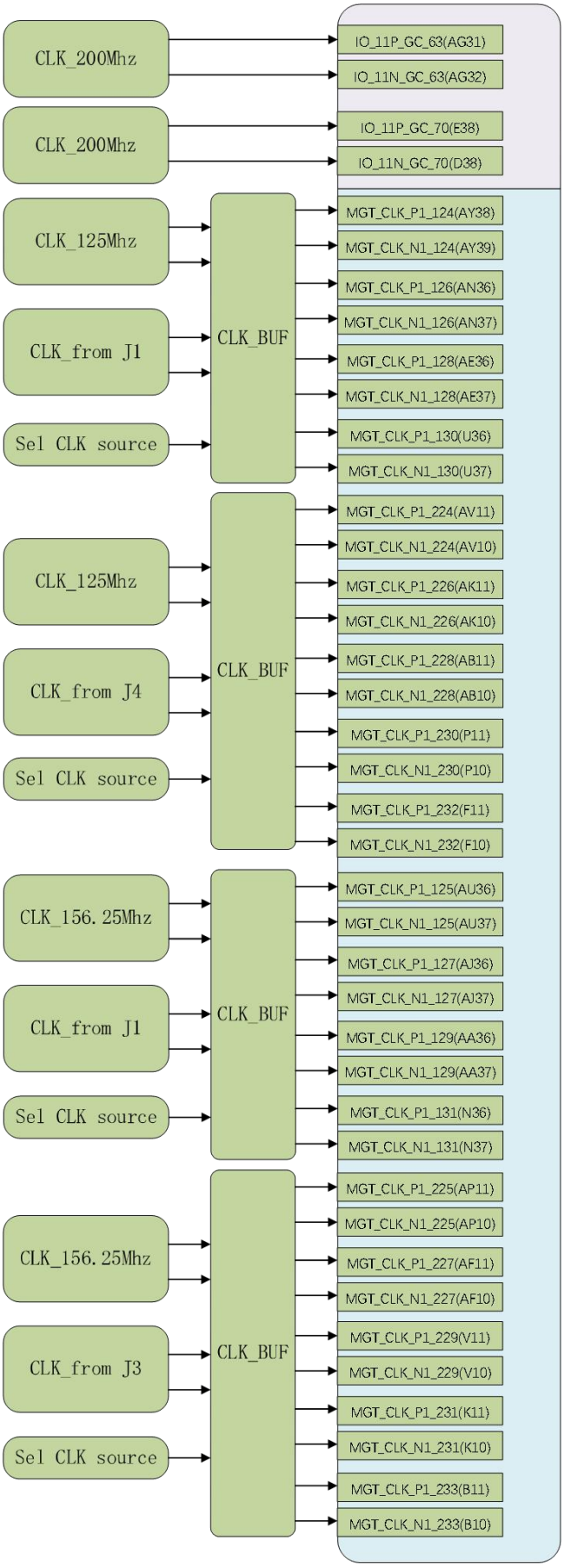
Due to the different logic usage of the core board, the limit current of the core board power supply is 20A, so the external power supply needs to consider the limit current situation to ensure that the core board works stably.

Power supply output voltage to the module needs to be stable, and need to consider the power surge, the core board power input port needs to add a few large capacitors (220Uf/25V), such as the cost allows, you can add a level of DC2DC chip, to ensure that the power supply is stable.



Part 3.4: SOM Clock

The SOM core board provides multiple differential clocks with frequencies of 200M/125M/156.25M to meet various application requirements. In addition, 125M/156.25M clock also added a clock buffer, can be achieved on-board clock and external clock input switching. When the clock select signal is grounded the clock source is a differential crystal, when the clock select signal is not grounded the clock source is an external input from the connector. The following diagram lists the clock connections in detail and pin locations, for a more detailed description, please refer to the core board schematic.


CLK_200Mhz
CLK_200Mhz
CLK_125Mhz
CLK_from J1
Sel CLK source
CLK_BUF
CLK_125Mhz
CLK_from J4
Sel CLK source
CLK_BUF
CLK_156.25Mhz
CLK_from J1
Sel CLK source
CLK_BUF
CLK_156.25Mhz
CLK_from J3
Sel CLK source
CLK_BUF
IO_11P_GC_63(AG31)
IO_11N_GC_63(AG32)
IO_11P_GC_70(E38)
IO_11N_GC_70(D38)
MGT_CLK_P1_124(AY38)
MGT_CLK_N1_124(AY39)
MGT_CLK_P1_126(AN36)
MGT_CLK_N1_126(AN37)
MGT_CLK_P1_128(AE36)
MGT_CLK_N1_128(AE37)
MGT_CLK_P1_130(U36)
MGT_CLK_N1_130(U37)
MGT_CLK_P1_224(AV11)
MGT_CLK_N1_224(AV10)
MGT_CLK_P1_226(AK11)
MGT_CLK_N1_226(AK10)
MGT_CLK_P1_228(AB11)
MGT_CLK_N1_228(AB10)
MGT_CLK_P1_230(P11)
MGT_CLK_N1_230(P10)
MGT_CLK_P1_232(F11)
MGT_CLK_N1_232(F10)
MGT_CLK_P1_125(AU36)
MGT_CLK_N1_125(AU37)
MGT_CLK_P1_127(AJ36)
MGT_CLK_N1_127(AJ37)
MGT_CLK_P1_129(AA36)
MGT_CLK_N1_129(AA37)
MGT_CLK_P1_131(N36)
MGT_CLK_N1_131(N37)
MGT_CLK_P1_225(AP11)
MGT_CLK_N1_225(AP10)
MGT_CLK_P1_227(AF11)
MGT_CLK_N1_227(AF10)
MGT_CLK_P1_229(V11)
MGT_CLK_N1_229(V10)
MGT_CLK_P1_231(K11)
MGT_CLK_N1_231(K10)
MGT_CLK_P1_233(B11)
MGT_CLK_N1_233(B10)

Part 3.5: SOM Reset Key

Considering the maximum retention of IO ports lead to the carrier board, the core board does not add a reset key, in the carrier board we reserved a reset key. The user can also select the IO as the reset signal according to the requirement.

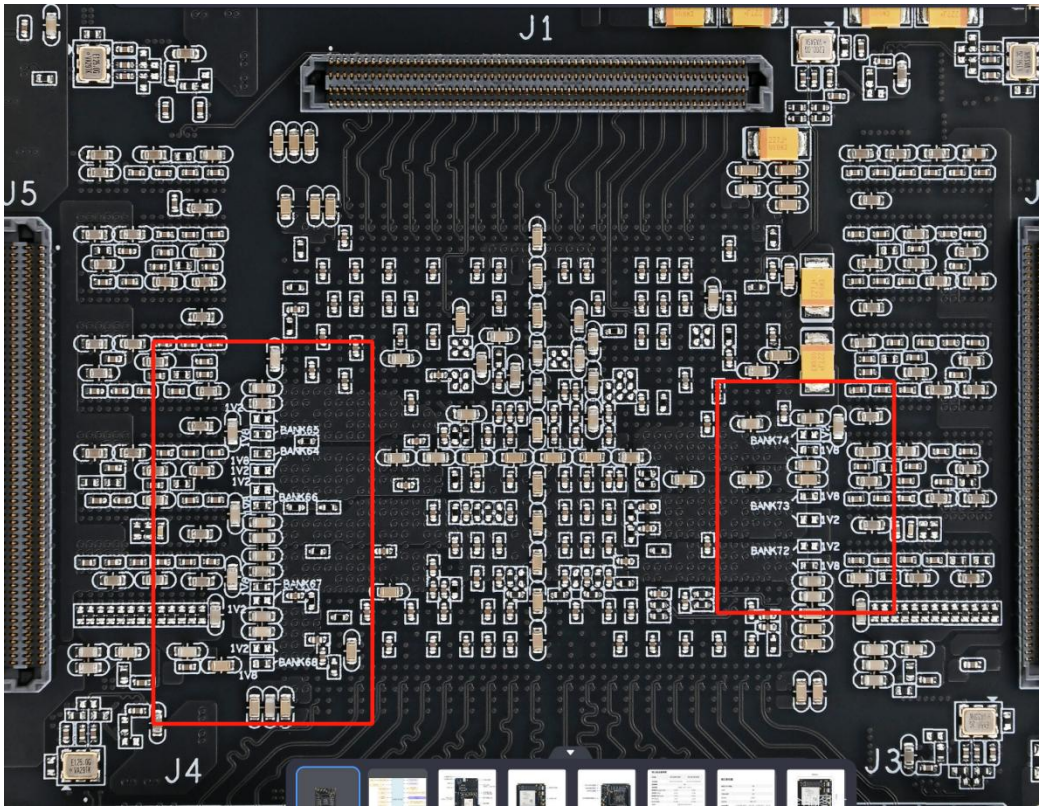
Part 3.6: Boot Mode Selection

The boot mode selection pins **BOOT_M2/BOOT_M1/BOOT_M0** of the main chip are pinned out to the SOM core board connector, and the user can select the corresponding boot mode through the three pins, and the mainstream boot modes are **JTAG**, **QSPI Flash**, and **BPI Flash** respectively. FPGA development board we reserved JTAG, QSPI Flash two start-up mode, more detailed description can refer to the SOM core board schematic.

The BOOT_M2/BOOT_M1/BOOT_M0 level standard is 1.8V.

Part 3.7: BANK Interface Level Selection

Th BANK64/65/66/67/68/72/73/74 on the SOM core board are all HP BANKs, the interface level is configured as 1.2/1.8V, and the voltage can be adjusted by selecting the resistor position through the instructions provided on the FPGA Carrier board, the default level is 1.8V. The corresponding resistors are label as shown in the figure below.



Part 3.8: Dual Group of DDR4 (8GB+8GB)

The SOM is configured with two group of DDR4, each group of four industrial-grade DDR4 chip, single capacity of 2GB, four total capacity of 8GB, dual-group DDR4 total capacity of 16GB, two groups of DDR4 pin assignment see the table below, , for more detailed information, please refer to the core board schematic.

DDR4 Pin	Pin Name	Pin Position
1_DDR4_DQ0	IO_L6P_T0U_N10_AD6P_61	BC29
1_DDR4_DQ1	IO_L2N_T0L_N3_61	BE32
1_DDR4_DQ2	IO_L3P_T0L_N4_AD15P_61	BE30
1_DDR4_DQ3	IO_L5P_T0U_N8_AD14P_61	BD33
1_DDR4_DQ4	IO_L6N_T0U_N11_AD6N_61	BD29
1_DDR4_DQ5	IO_L5N_T0U_N9_AD14N_61	BE33
1_DDR4_DQ6	IO_L3N_T0L_N5_AD15N_61	BF30
1_DDR4_DQ7	IO_L2P_T0L_N2_61	BE31
1_DDR4_DM0	IO_L1P_T0L_N0_DBC_61	BF32
1_DDR4_DQS_P0	IO_L4P_T0U_N6_DBC_AD7P_61	BD30
1_DDR4_DQS_N0	IO_L4N_T0U_N7_DBC_AD7N_61	BD31
1_DDR4_DQ8	IO_L11P_T1U_N8_GC_61	AY30
1_DDR4_DQ9	IO_L8P_T1L_N2_AD5P_61	BB30
1_DDR4_DQ10	IO_L11N_T1U_N9_GC_61	BA30
1_DDR4_DQ11	IO_L9N_T1L_N5_AD12N_61	BB29
1_DDR4_DQ12	IO_L12P_T1U_N10_GC_61	AY31
1_DDR4_DQ13	IO_L8N_T1L_N3_AD5N_61	BB31
1_DDR4_DQ14	IO_L9P_T1L_N4_AD12P_61	BA29
1_DDR4_DQ15	IO_L12N_T1U_N11_GC_61	AY32
1_DDR4_DM1	IO_L7P_T1L_N0_QBC_AD13P_61	BC31
1_DDR4_DQS_P1	IO_L10P_T1U_N6_QBC_AD4P_61	BA32
1_DDR4_DQS_N1	IO_L10N_T1U_N7_QBC_AD4N_61	BB32
1_DDR4_DQ16	IO_L18N_T2U_N11_AD2N_61	AT30
1_DDR4_DQ17	IO_L17N_T2U_N9_AD10N_61	AU31
1_DDR4_DQ18	IO_L17P_T2U_N8_AD10P_61	AU30
1_DDR4_DQ19	IO_L15P_T2L_N4_AD11P_61	AU32
1_DDR4_DQ20	IO_L18P_T2U_N10_AD2P_61	AT29
1_DDR4_DQ21	IO_L14N_T2L_N3_GC_61	AW31
1_DDR4_DQ22	IO_L14P_T2L_N2_GC_61	AV31
1_DDR4_DQ23	IO_L15N_T2L_N5_AD11N_61	AV32
1_DDR4_DM2	IO_L13P_T2L_N0_GC_QBC_61	AW29
1_DDR4_DQS_P2	IO_L16P_T2U_N6_QBC_AD3P_61	AU29
1_DDR4_DQS_N2	IO_L16N_T2U_N7_QBC_AD3N_61	AV29
1_DDR4_DQ24	IO_L24P_T3U_N10_61	AL29
1_DDR4_DQ25	IO_L21N_T3L_N5_AD8N_61	AP29

1_DDR4_DQ26	IO_L23P_T3U_N8_61	AM31
1_DDR4_DQ27	IO_L20P_T3L_N2_AD1P_61	AP30
1_DDR4_DQ28	IO_L24N_T3U_N11_61	AL30
1_DDR4_DQ29	IO_L23N_T3U_N9_61	AN31
1_DDR4_DQ30	IO_L21P_T3L_N4_AD8P_61	AN29
1_DDR4_DQ31	IO_L20N_T3L_N3_AD1N_61	AR30
1_DDR4_DM3	IO_L19P_T3L_N0_DBC_AD9P_61	AP31
1_DDR4_DQS_P3	IO_L22P_T3U_N6_DBC_AD0P_61	AM29
1_DDR4_DQS_N3	IO_L22N_T3U_N7_DBC_AD0N_61	AM30
1_DDR4_DQ32	IO_L6N_T0U_N11_AD6N_62	BC38
1_DDR4_DQ33	IO_L2P_T0L_N2_62	BE38
1_DDR4_DQ34	IO_L3N_T0L_N5_AD15N_62	BF37
1_DDR4_DQ35	IO_L5N_T0U_N9_AD14N_62	BD39
1_DDR4_DQ36	IO_L6P_T0U_N10_AD6P_62	BB38
1_DDR4_DQ37	IO_L5P_T0U_N8_AD14P_62	BC39
1_DDR4_DQ38	IO_L3P_T0L_N4_AD15P_62	BE37
1_DDR4_DQ39	IO_L2N_T0L_N3_62	BF38
1_DDR4_DM4	IO_L1P_T0L_N0_DBC_62	BF39
1_DDR4_DQS_P4	IO_L4P_T0U_N6_DBC_AD7P_62	BD40
1_DDR4_DQS_N4	IO_L4N_T0U_N7_DBC_AD7N_62	BE40
1_DDR4_DQ40	IO_L12N_T1U_N11_GC_62	BB35
1_DDR4_DQ41	IO_L11P_T1U_N8_GC_62	BB36
1_DDR4_DQ42	IO_L8P_T1L_N2_AD5P_62	BD35
1_DDR4_DQ43	IO_L9N_T1L_N5_AD12N_62	BE36
1_DDR4_DQ44	IO_L12P_T1U_N10_GC_62	BA35
1_DDR4_DQ45	IO_L9P_T1L_N4_AD12P_62	BD36
1_DDR4_DQ46	IO_L8N_T1L_N3_AD5N_62	BE35
1_DDR4_DQ47	IO_L11N_T1U_N9_GC_62	BC36
1_DDR4_DM5	IO_L7P_T1L_N0_QBC_AD13P_62	BC34
1_DDR4_DQS_P5	IO_L10P_T1U_N6_QBC_AD4P_62	BB37
1_DDR4_DQS_N5	IO_L10N_T1U_N7_QBC_AD4N_62	BC37
1_DDR4_DQ48	IO_L14N_T2L_N3_GC_62	AY36
1_DDR4_DQ49	IO_L17N_T2U_N9_AD10N_62	AW34
1_DDR4_DQ50	IO_L14P_T2L_N2_GC_62	AY35
1_DDR4_DQ51	IO_L18N_T2U_N11_AD2N_62	AW33
1_DDR4_DQ52	IO_L15P_T2L_N4_AD11P_62	AY33
1_DDR4_DQ53	IO_L17P_T2U_N8_AD10P_62	AV34
1_DDR4_DQ54	IO_L15N_T2L_N5_AD11N_62	BA33
1_DDR4_DQ55	IO_L18P_T2U_N10_AD2P_62	AV33
1_DDR4_DM6	IO_L13P_T2L_N0_GC_QBC_62	BA34
1_DDR4_DQS_P6	IO_L16P_T2U_N6_QBC_AD3P_62	AW35
1_DDR4_DQS_N6	IO_L16N_T2U_N7_QBC_AD3N_62	AW36

1_DDR4_DQ56	IO_L21P_T3L_N4_AD8P_62	AN34
1_DDR4_DQ57	IO_L24N_T3U_N11_62	AM34
1_DDR4_DQ58	IO_L21N_T3L_N5_AD8N_62	AP34
1_DDR4_DQ59	IO_L23N_T3U_N9_62	AM32
1_DDR4_DQ60	IO_L20P_T3L_N2_AD1P_62	AP33
1_DDR4_DQ61	IO_L24P_T3U_N10_62	AL34
1_DDR4_DQ62	IO_L20N_T3L_N3_AD1N_62	AR33
1_DDR4_DQ63	IO_L23P_T3U_N8_62	AL32
1_DDR4_DM7	IO_L19P_T3L_N0_DBC_AD9P_62	AT33
1_DDR4_DQS_P7	IO_L22P_T3U_N6_DBC_AD0P_62	AN32
1_DDR4_DQS_N7	IO_L22N_T3U_N7_DBC_AD0N_62	AN33
1_DDR4_A0	IO_L5N_T0U_N9_AD14N_63	AG30
1_DDR4_A1	IO_L20N_T3L_N3_AD1N_63	AB34
1_DDR4_A2	IO_L16N_T2U_N7_QBC_AD3N_63	AD31
1_DDR4_A3	IO_L18P_T2U_N10_AD2P_63	AC34
1_DDR4_A4	IO_L5P_T0U_N8_AD14P_63	AG29
1_DDR4_A5	IO_L19N_T3L_N1_DBC_AD9N_63	AA33
1_DDR4_A6	IO_L4P_T0U_N6_DBC_AD7P_63	AH28
1_DDR4_A7	IO_L20P_T3L_N2_AD1P_63	AA34
1_DDR4_A8	IO_L2P_T0L_N2_63	AJ28
1_DDR4_A9	IO_L16P_T2U_N6_QBC_AD3P_63	AC31
1_DDR4_A10	IO_L3N_T0L_N5_AD15N_63	AJ30
1_DDR4_A11	IO_L2N_T0L_N3_63	AK28
1_DDR4_A12	IO_L18N_T2U_N11_AD2N_63	AD34
1_DDR4_A13	IO_L21P_T3L_N4_AD8P_63	W30
1_DDR4_A14	IO_L6P_T0U_N10_AD6P_63	AJ31
1_DDR4_A15	IO_L19P_T3L_N0_DBC_AD9P_63	AA32
1_DDR4_A16	IO_L17P_T2U_N8_AD10P_63	AC32
1_DDR4_A17	IO_L13N_T2L_N1_GC_QBC_63	AE32
1_DDR4_BA0	IO_L3P_T0L_N4_AD15P_63	AJ29
1_DDR4_BA1	IO_L14P_T2L_N2_GC_63	AD33
1_DDR4_BG0	IO_L15N_T2L_N5_AD11N_63	AF30
1_DDR4_nCS	IO_T2U_N12_63	AD30
1_DDR4_ODT	IO_L7P_T1L_N0_QBC_AD13P_63	AH34
1_DDR4_nRESET	IO_T1U_N12_63	AK32
1_DDR4_CLK_P	IO_L12P_T1U_N10_GC_63	AF32
1_DDR4_CLK_N	IO_L12N_T1U_N11_GC_63	AF33
1_DDR4_CKE	IO_L7N_T1L_N1_QBC_AD13N_63	AJ34
1_DDR4_TEN	IO_T3U_N12_63	AB32
1_DDR4_nACT	IO_L14N_T2L_N3_GC_63	AE33
1_DDR4_nALERT	IO_L17N_T2U_N9_AD10N_63	AC33
1_DDR4_PARITY	IO_L8P_T1L_N2_AD5P_63	AH33

DDR4 Pin	Pin Name	Pin Position
2_DDR4_DQ0	IO_L5P_T0U_N8_AD14P_69	V31
2_DDR4_DQ1	IO_L5N_T0U_N9_AD14N_69	U31
2_DDR4_DQ2	IO_L2P_T0L_N2_69	T33
2_DDR4_DQ3	IO_L3N_T0L_N5_AD15N_69	T32
2_DDR4_DQ4	IO_L3P_T0L_N4_AD15P_69	U32
2_DDR4_DQ5	IO_L6P_T0U_N10_AD6P_69	U30
2_DDR4_DQ6	IO_L2N_T0L_N3_69	R33
2_DDR4_DQ7	IO_L6N_T0U_N11_AD6N_69	T30
2_DDR4_DM0	IO_L1P_T0L_N0_DBC_69	U34
2_DDR4_DQS_P0	IO_L4P_T0U_N6_DBC_AD7P_69	V32
2_DDR4_DQS_N0	IO_L4N_T0U_N7_DBC_AD7N_69	V33
2_DDR4_DQ8	IO_L9N_T1L_N5_AD12N_69	N34
2_DDR4_DQ9	IO_L8P_T1L_N2_AD5P_69	R31
2_DDR4_DQ10	IO_L9P_T1L_N4_AD12P_69	P34
2_DDR4_DQ11	IO_L12P_T1U_N10_GC_69	N32
2_DDR4_DQ12	IO_L8N_T1L_N3_AD5N_69	R32
2_DDR4_DQ13	IO_L11P_T1U_N8_GC_69	P31
2_DDR4_DQ14	IO_L12N_T1U_N11_GC_69	N33
2_DDR4_DQ15	IO_L11N_T1U_N9_GC_69	N31
2_DDR4_DM1	IO_L7P_T1L_N0_QBC_AD13P_69	R30
2_DDR4_DQS_P1	IO_L10P_T1U_N6_QBC_AD4P_69	M34
2_DDR4_DQS_N1	IO_L10N_T1U_N7_QBC_AD4N_69	L34
2_DDR4_DQ16	IO_L18P_T2U_N10_AD2P_69	L33
2_DDR4_DQ17	IO_L15P_T2L_N4_AD11P_69	M30
2_DDR4_DQ18	IO_L14P_T2L_N2_GC_69	L32
2_DDR4_DQ19	IO_L17P_T2U_N8_AD10P_69	K31
2_DDR4_DQ20	IO_L15N_T2L_N5_AD11N_69	L30
2_DDR4_DQ21	IO_L17N_T2U_N9_AD10N_69	J31
2_DDR4_DQ22	IO_L18N_T2U_N11_AD2N_69	K33
2_DDR4_DQ23	IO_L14N_T2L_N3_GC_69	K32
2_DDR4_DM2	IO_L13P_T2L_N0_GC_QBC_69	M31
2_DDR4_DQS_P2	IO_L16P_T2U_N6_QBC_AD3P_69	K30
2_DDR4_DQS_N2	IO_L16N_T2U_N7_QBC_AD3N_69	J30
2_DDR4_DQ24	IO_L24P_T3U_N10_69	F33
2_DDR4_DQ25	IO_L23N_T3U_N9_69	E32
2_DDR4_DQ26	IO_L21N_T3L_N5_AD8N_69	G32
2_DDR4_DQ27	IO_L24N_T3U_N11_69	E33
2_DDR4_DQ28	IO_L21P_T3L_N4_AD8P_69	H32
2_DDR4_DQ29	IO_L23P_T3U_N8_69	F32
2_DDR4_DQ30	IO_L20P_T3L_N2_AD1P_69	H31
2_DDR4_DQ31	IO_L20N_T3L_N3_AD1N_69	G31

2_DDR4_DM3	IO_L19P_T3L_N0_DBC_AD9P_69	G30
2_DDR4_DQS_P3	IO_L22P_T3U_N6_DBC_AD0P_69	J33
2_DDR4_DQS_N3	IO_L22N_T3U_N7_DBC_AD0N_69	H33
2_DDR4_DQ32	IO_L6P_T0U_N10_AD6P_71	P26
2_DDR4_DQ33	IO_L3P_T0L_N4_AD15P_71	T26
2_DDR4_DQ34	IO_L6N_T0U_N11_AD6N_71	N26
2_DDR4_DQ35	IO_L2N_T0L_N3_71	R27
2_DDR4_DQ36	IO_L5P_T0U_N8_AD14P_71	P28
2_DDR4_DQ37	IO_L2P_T0L_N2_71	T27
2_DDR4_DQ38	IO_L5N_T0U_N9_AD14N_71	N28
2_DDR4_DQ39	IO_L3N_T0L_N5_AD15N_71	R26
2_DDR4_DM4	IO_L1P_T0L_N0_DBC_71	T28
2_DDR4_DQS_P4	IO_L4P_T0U_N6_DBC_AD7P_71	P29
2_DDR4_DQS_N4	IO_L4N_T0U_N7_DBC_AD7N_71	N29
2_DDR4_DQ40	IO_L12P_T1U_N10_GC_71	J28
2_DDR4_DQ41	IO_L9P_T1L_N4_AD12P_71	M27
2_DDR4_DQ42	IO_L11P_T1U_N8_GC_71	H27
2_DDR4_DQ43	IO_L8P_T1L_N2_AD5P_71	L28
2_DDR4_DQ44	IO_L11N_T1U_N9_GC_71	H28
2_DDR4_DQ45	IO_L9N_T1L_N5_AD12N_71	L27
2_DDR4_DQ46	IO_L12N_T1U_N11_GC_71	J29
2_DDR4_DQ47	IO_L8N_T1L_N3_AD5N_71	K28
2_DDR4_DM5	IO_L7P_T1L_N0_QBC_AD13P_71	M29
2_DDR4_DQS_P5	IO_L10P_T1U_N6_QBC_AD4P_71	K26
2_DDR4_DQS_N5	IO_L10N_T1U_N7_QBC_AD4N_71	K27
2_DDR4_DQ48	IO_L18N_T2U_N11_AD2N_71	D28
2_DDR4_DQ49	IO_L17N_T2U_N9_AD10N_71	E27
2_DDR4_DQ50	IO_L18P_T2U_N10_AD2P_71	E28
2_DDR4_DQ51	IO_L17P_T2U_N8_AD10P_71	F27
2_DDR4_DQ52	IO_L15N_T2L_N5_AD11N_71	G29
2_DDR4_DQ53	IO_L14N_T2L_N3_GC_71	G27
2_DDR4_DQ54	IO_L15P_T2L_N4_AD11P_71	H29
2_DDR4_DQ55	IO_L14P_T2L_N2_GC_71	G26
2_DDR4_DM6	IO_L13P_T2L_N0_GC_QBC_71	J26
2_DDR4_DQS_P6	IO_L16P_T2U_N6_QBC_AD3P_71	F28
2_DDR4_DQS_N6	IO_L16N_T2U_N7_QBC_AD3N_71	F29
2_DDR4_DQ56	IO_L23P_T3U_N8_71	B29
2_DDR4_DQ57	IO_L21N_T3L_N5_AD8N_71	D30
2_DDR4_DQ58	IO_L24P_T3U_N10_71	B30
2_DDR4_DQ59	IO_L20N_T3L_N3_AD1N_71	C29
2_DDR4_DQ60	IO_L23N_T3U_N9_71	A29
2_DDR4_DQ61	IO_L21P_T3L_N4_AD8P_71	E30

2_DDR4_DQ62	IO_L24N_T3U_N11_71	A30
2_DDR4_DQ63	IO_L20P_T3L_N2_AD1P_71	D29
2_DDR4_DM7	IO_L19P_T3L_N0_DBC_AD9P_71	C27
2_DDR4_DQS_P7	IO_L22P_T3U_N6_DBC_AD0P_71	A27
2_DDR4_DQS_N7	IO_L22N_T3U_N7_DBC_AD0N_71	A28
2_DDR4_A0	IO_L5P_T0U_N8_AD14P_70	H34
2_DDR4_A1	IO_L6P_T0U_N10_AD6P_70	F34
2_DDR4_A2	IO_L13N_T2L_N1_GC_QBC_70	C37
2_DDR4_A3	IO_L17P_T2U_N8_AD10P_70	B35
2_DDR4_A4	IO_L2P_T0L_N2_70	G37
2_DDR4_A5	IO_L19N_T3L_N1_DBC_AD9N_70	A34
2_DDR4_A6	IO_L3N_T0L_N5_AD15N_70	J36
2_DDR4_A7	IO_L19P_T3L_N0_DBC_AD9P_70	B34
2_DDR4_A8	IO_L5N_T0U_N9_AD14N_70	G34
2_DDR4_A9	IO_L20N_T3L_N3_AD1N_70	C34
2_DDR4_A10	IO_L2N_T0L_N3_70	F37
2_DDR4_A11	IO_L18P_T2U_N10_AD2P_70	E35
2_DDR4_A12	IO_L16N_T2U_N7_QBC_AD3N_70	B37
2_DDR4_A13	IO_L20P_T3L_N2_AD1P_70	D34
2_DDR4_A14	IO_L4P_T0U_N6_DBC_AD7P_70	H36
2_DDR4_A15	IO_L18N_T2U_N11_AD2N_70	D35
2_DDR4_A16	IO_L16P_T2U_N6_QBC_AD3P_70	B36
2_DDR4_A17	IO_L21P_T3L_N4_AD8P_70	D33
2_DDR4_BA0	IO_T2U_N12_70	E37
2_DDR4_BA1	IO_L14N_T2L_N3_GC_70	D36
2_DDR4_BG0	IO_L7P_T1L_N0_QBC_AD13P_70	E40
2_DDR4_NCS	IO_L14P_T2L_N2_GC_70	E36
2_DDR4_ODT	IO_T1U_N12_70	F38
2_DDR4_nRESET	IO_L15N_T2L_N5_AD11N_70	A38
2_DDR4_CLK_P	IO_L12P_T1U_N10_GC_70	C38
2_DDR4_CLK_N	IO_L12N_T1U_N11_GC_70	C39
2_DDR4_CKE	IO_L7N_T1L_N1_QBC_AD13N_70	D40
2_DDR4_TEN	IO_L3P_T0L_N4_AD15P_70	J35
2_DDR4_nACT	IO_L8P_T1L_N2_AD5P_70	E39
2_DDR4_nALERT	IO_T3U_N12_70	B31
2_DDR4_PARITY	IO_L17N_T2U_N9_AD10N_70	A35

Part 3.9: SOM Signals with Equal Length

The signals leading out of the core board to the connector on the carrier are made strictly equal length, you can refer to the signal equal length table provided, which lists the signal names

and signal alignment lengths in detail, and the table has been stored under the corresponding folder.

Part 3.10: Core Board Package Library

In order to facilitate the user to quickly use the core board, we provide the corresponding package library, the relative position of the connector and the core board frame silkscreen have been placed, you can directly call to use it.

The schematic package provides two versions of AD/ORCAD, and the PCB package provides two versions of AD/Allegro, which are stored in the corresponding folder.

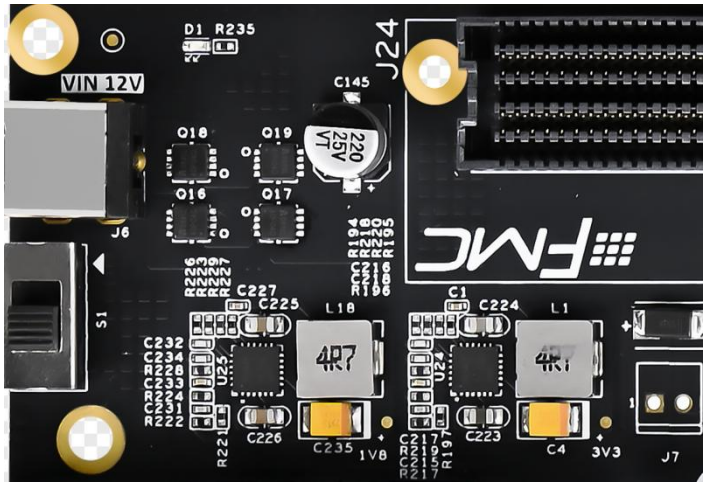
Part 3.11: Core Board Connectors

The core board is connected to the carrier board via two 0.5mm/168P gold-plated high-speed connectors on the bottom. The connector model used on the carrier board is **ADM6-60-01.5-L-4-2-A-TR.**

Part 4: Carrier Board Overview

Part 4.1: Power Supply

The FPGA development board is powered by a 12V/20A adapter or by PCIE. The two power supplies can be switched via the S1 switch. After the power supply is connected, it is converted into 3.3V, 1.8V and other multi-channel voltages through DCDC for use by the devices on the board. the detailed circuit of the power supply part can refer to the corresponding schematic of the FPGA development board



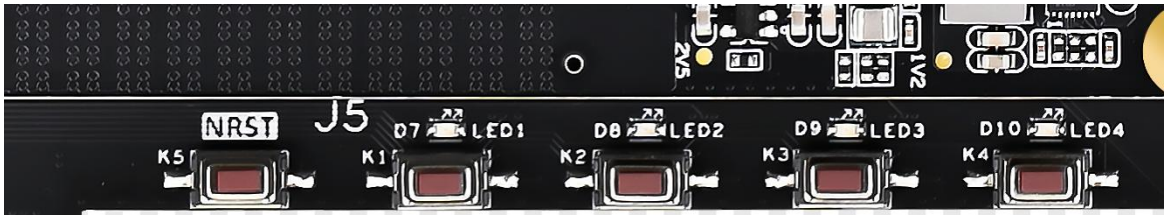
Part 4.2: System Clock

The clock circuit is mainly on the core board, you can refer to the core board clock section for reference

Part 4.3: System Reset

One Reset key is reserved on the FPGA carrier board. The key is high by default and low when pressed.

The reset pin is connected to the IO_2P_68(BE8) pin of the BANK68 with a level of 1.8V. For detailed circuitry of the reset part, please refer to the schematic of the FPGA development board.



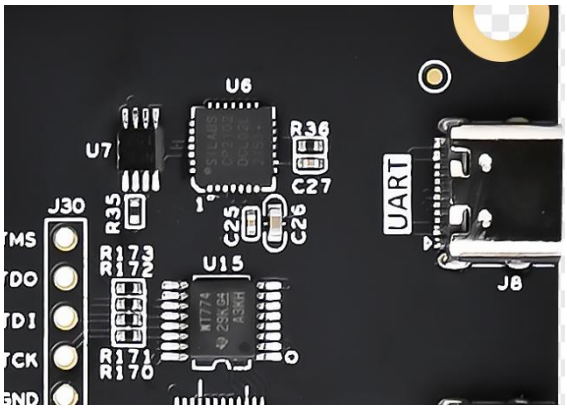
Part 4.4: USB to UART

The FPGA carrier board uses "**Silicon Labs CP2102GM**" chip to realize USB to UART, and the USB interface adopts "**Micro USB**". Users only need to use a Micro USB cable to connect to the PC for serial communication.

The "**TX/RX**" signal of the UART is connected with the "**BANK86**" of the "**FPGA**", and the interface level is 1.8V, so the serial port interface adopts the level conversion to 3.3V and connects with the serial port chip.

The following is the signal correspondence table and schematic, the TX/RX direction is defined by the FPGA side.

UART0 Pin	Pin Name	Pin Position
UART_TX	IO_9P_68	BC8
UART_RX	IO_9N_68	BC7

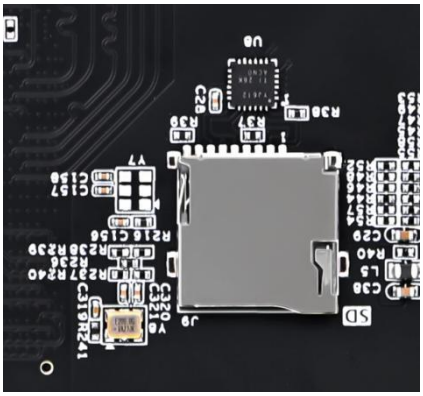


Part 4.5: SD Card Slot Interface

The SD card holder (Backside of the FPGA board) is placed on the board, you can do SD card startup, but also convenient for users to debug or users to do file storage, the circuit interface level is 1.8V, SD card signals are connected to the BANK67 of FPGA, TF card level IS 3.3V, through the special level converter chip to achieve the SD card signal 1.8V to 3.3V.

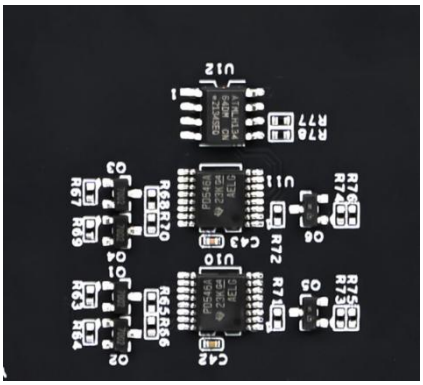
The following is the correspondence of the signals, the detailed circuit can be referred to the schematic diagram of the development board.

SD Card Slot	Pin Name	Pin Position
SD-CLK	IO_20P_67	AP15
SD-CMD	IO_20N_67	AP14
SD-DATA0	IO_21P_67	AN14
SD-DATA1	IO_21N_67	AN13
SD-DATA2	IO_24P_67	AL14
SD-DATA3	IO_24N_67	AM14



Part 4.6: E2PROM

The **64Kbit EEPROM** chip is placed on the FPGA carrier board, the model is AT24C64D-SSHM-T Connect with **BANK68** of **FPGA** through **IIC** bus. The **EEPROM** read address is **0xA1**, and the write address is **0xA0**. The following is the pin assignment of the **EEPROM**, the detailed circuit can refer to the schematic diagram of the development board.

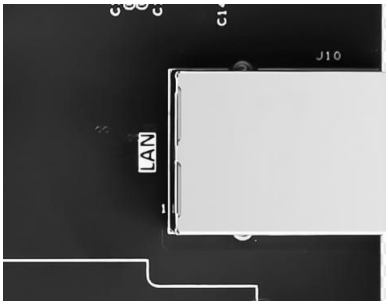


Part 4.7: Gigabit Ethernet

The FPGA carrier board is designed with one way Gigabit Ethernet. The Ethernet chip and **FPGA** are interconnected through the **RGMII** interface. Connect the corresponding pins as shown in the table below, the address of the network port is **PHY_AD[2:0]=001**, you can refer to the schematic for the detailed circuit.

RMGII Signal	Pin Name	Pin Position
GTX_CLK	IO_10P_67	BB15
TXD0	IO_7P_67	BA12
TXD1	IO_7N_67	BB12
TXD2	IO_8P_67	AY12
TXD3	IO_8N_67	AY11
TX_EN	IO_10N_67	BB14

RX_CLK	IO_14P_GC_67	AW16
RXD0	IO_2P_67	BE15
RXD1	IO_2N_67	BF15
RXD2	IO_5P_67	BD15
RXD3	IO_5N_67	BD14
RX_DV	IO_14N_GC_67	AW15
MDC	IO_6P_67	BC14
MDIO	IO_6N_67	BC13



Part 4.8: QSFP28 Interface

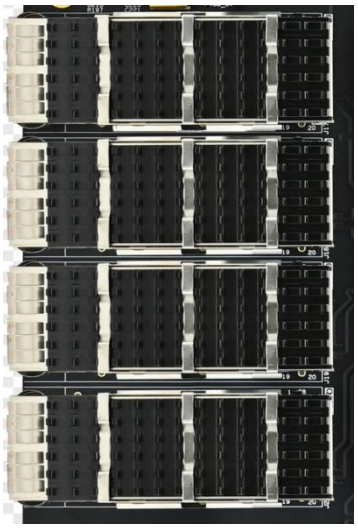
Four 100G QSFP28 interfaces are designed on the FPGA carrier board. The interface signals are connected to the BANK94/BANK128 of the FPGA. For details, please refer to the schematic.

The following is the pin assignment of **QSFP**, the detailed circuit can refer to the schematic of the FPGA development board.

QSFP1 Pin	Pin Name	Pin Position	QSFP2 Pin	Pin Name	Pin Position
QSFP1-TX-P0	MGT_TX_P0_230	U9	QSFP2-TX-P0	MGT_TX_P0_229	AA9
QSFP1-TX-N0	MGT_TX_N0_230	U8	QSFP2-TX-N0	MGT_TX_N0_229	AA8
QSFP1-TX-P1	MGT_TX_P1_230	T7	QSFP2-TX-P1	MGT_TX_P1_229	Y7
QSFP1-TX-N1	MGT_TX_N1_230	T6	QSFP2-TX-N1	MGT_TX_N1_229	Y6
QSFP1-TX-P2	MGT_TX_P2_230	R9	QSFP2-TX-P2	MGT_TX_P2_229	W9
QSFP1-TX-N2	MGT_TX_N2_230	R8	QSFP2-TX-N2	MGT_TX_N2_229	W8
QSFP1-TX-P3	MGT_TX_P3_230	P7	QSFP2-TX-P3	MGT_TX_P3_229	V7
QSFP1-TX-N3	MGT_TX_N3_230	P6	QSFP2-TX-N3	MGT_TX_N3_229	V6
QSFP1-RX-P0	MGT_RX_P0_230	U4	QSFP2-RX-P0	MGT_RX_P0_229	AA4
QSFP1-RX-N0	MGT_RX_N0_230	U3	QSFP2-RX-N0	MGT_RX_N0_229	AA3
QSFP1-RX-P1	MGT_RX_P1_230	T2	QSFP2-RX-P1	MGT_RX_P1_229	Y2
QSFP1-RX-N1	MGT_RX_N1_230	T1	QSFP2-RX-N1	MGT_RX_N1_229	Y1
QSFP1-RX-P2	MGT_RX_P2_230	R4	QSFP2-RX-P2	MGT_RX_P2_229	W4
QSFP1-RX-N2	MGT_RX_N2_230	R3	QSFP2-RX-N2	MGT_RX_N2_229	W3
QSFP1-RX-P3	MGT_RX_P3_230	P2	QSFP2-RX-P3	MGT_RX_P3_229	V2
QSFP1-RX-N3	MGT_RX_N3_230	P1	QSFP2-RX-N3	MGT_RX_N3_229	V1
QSFP1_LPMODE	IO_3P_68	BF10	QSFP2_LPMODE	IO_3N_68	BF9

QSFP1_I2C_SCL	IIC Expansion Chip, Refer to Schematic	QSFP2_I2C_SCL	IIC Expansion Chip, Refer to Schematic
QSFP1_I2C_SDA	IIC Expansion Chip, Refer to Schematic	QSFP2_I2C_SDA	IIC Expansion Chip, Refer to Schematic

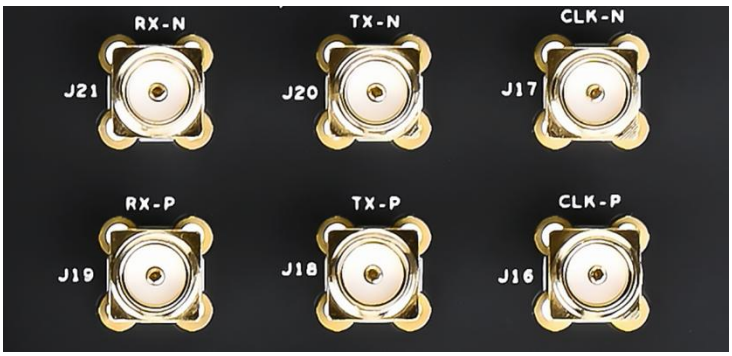
QSFP3 Pin	Pin Name	Pin Position	QSFP4 Pin	Pin Name	Pin Position
QSFP3-TX-P0	MGT_TX_P0_228	AE9	QSFP4-TX-P0	MGT_TX_P0_227	AJ9
QSFP3-TX-N0	MGT_TX_N0_228	AE8	QSFP4-TX-N0	MGT_TX_N0_227	AJ8
QSFP3-TX-P1	MGT_TX_P1_228	AD7	QSFP4-TX-P1	MGT_TX_P1_227	AH7
QSFP3-TX-N1	MGT_TX_N1_228	AD6	QSFP4-TX-N1	MGT_TX_N1_227	AH6
QSFP3-TX-P2	MGT_TX_P2_228	AC9	QSFP4-TX-P2	MGT_TX_P2_227	AG9
QSFP3-TX-N2	MGT_TX_N2_228	AC8	QSFP4-TX-N2	MGT_TX_N2_227	AG8
QSFP3-TX-P3	MGT_TX_P3_228	AB7	QSFP4-TX-P3	MGT_TX_P3_227	AF7
QSFP3-TX-N3	MGT_TX_N3_228	AB6	QSFP4-TX-N3	MGT_TX_N3_227	AF6
QSFP3-RX-P0	MGT_RX_P0_228	AE4	QSFP4-RX-P0	MGT_RX_P0_227	AJ4
QSFP3-RX-N0	MGT_RX_N0_228	AE3	QSFP4-RX-N0	MGT_RX_N0_227	AJ3
QSFP3-RX-P1	MGT_RX_P1_228	AD2	QSFP4-RX-P1	MGT_RX_P1_227	AH2
QSFP3-RX-N1	MGT_RX_N1_228	AD1	QSFP4-RX-N1	MGT_RX_N1_227	AH1
QSFP3-RX-P2	MGT_RX_P2_228	AC4	QSFP4-RX-P2	MGT_RX_P2_227	AG4
QSFP3-RX-N2	MGT_RX_N2_228	AC3	QSFP4-RX-N2	MGT_RX_N2_227	AG3
QSFP3-RX-P3	MGT_RX_P3_228	AB2	QSFP4-RX-P3	MGT_RX_P3_227	AF2
QSFP3-RX-N3	MGT_RX_N3_228	AB1	QSFP4-RX-N3	MGT_RX_N3_227	AF1
QSFP3_LPMODE	IO_6P_68	BD9	QSFP4_LPMODE	IO_6N_68	BD8
QSFP3_I2C_SCL	IIC Expansion Chip, Refer to Schematic		QSFP4_I2C_SCL	IIC Expansion Chip, Refer to Schematic	
QSFP3_I2C_SDA	IIC Expansion Chip, Refer to Schematic		QSFP4_I2C_SDA	IIC Expansion Chip, Refer to Schematic	



Part 4.9: SMA Interface

The FPGA carrier board is designed with six SMA interfaces connected to the MGT interface.The SMA pin locations are listed in the table below, the detailed circuit can refer to the schematic of the FPGA development board.

SMA Interface	Pin Name	Pin Position
MGT_CLK_P	MGT_CLK_P0_130	W36
MGT_CLK_N	MGT_CLK_N0_130	W37
MGT_TX_P	MGT_TX_P0_130	U40
MGT_TX_N	MGT_TX_N0_130	U41
MGT_RX_P	MGT_RX_P0_130	U45
MGT_RX_N	MGT_RX_N0_130	U46



Part 4.10: SATA Interface

The FPGA carrier board is designed with Four SATA interfaces.The pin locations are listed in the table below, the detailed circuit can refer to the schematic of the FPGA development board.

SATA1 Interface	Pin Name	Pin Position
SATA1_TX_P	MGT_TX_P0_131	N40
SATA1_TX_N	MGT_TX_N0_131	N41
SATA1_RX_P	MGT_RX_P0_131	N45
SATA1_RX_N	MGT_RX_N0_131	N46
SATA2 Interface	**Pin Name**	**Pin Position**
SATA2_TX_P	MGT_TX_P1_131	M38
SATA2_TX_N	MGT_TX_N1_131	M39
SATA2_RX_P	MGT_RX_P1_131	M43
SATA2_RX_N	MGT_RX_N1_131	M44
SATA3 Interface	**Pin Name**	**Pin Position**
SATA3_TX_P	MGT_TX_P2_131	L40
SATA3_TX_N	MGT_TX_N2_131	L41
SATA3_RX_P	MGT_RX_P2_131	L45
SATA3_RX_N	MGT_RX_N2_131	L46
SATA4 Interface	**Pin Name**	**Pin Position**

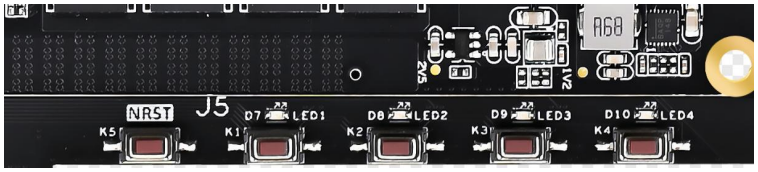
SATA4_TX_P	MGT_TX_P3_131	J40
SATA4_TX_N	MGT_TX_N3_131	J41
SATA4_RX_P	MGT_RX_P3_131	K43
SATA4_RX_N	MGT_RX_N3_131	K44



Part 4.11: LED

The core board is designed with three LEDs, and the FPGA Carrier Board is designed with four LEDs, totally seven LEDs. The LEDs are bright at high level and extinguished at low level. and you can refer to the schematic for Details.

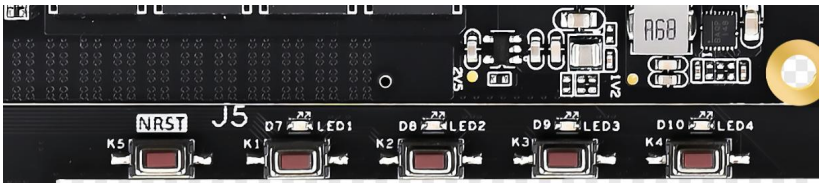
LED Bits	Pin Name	Pin Position
LED1	IO-5P-68	BE12
LED2	IO-5N-68	BF12
LED3	IO-4P-68	BE11
LED4	IO-4N-68	BE10



Part 4.12: KEY

Four **KEYs** are designed on the FPGA carrier board. The keys are high by default and low when pressed. The keys are connected to the PL side and the pin locations are listed in the table below

Key Bits	Pin Name	Pin Position
KEY1	IO-7P-68	BC12
KEY2	IO-7N-68	BC11
KEY3	IO-8P-68	BB11
KEY4	IO-8N-68	BB10



Part 4.13: FMC Expansion Port

Three **FMC** connectors are designed on the FPGA carrier board, one FMC HPC, two FMC LPC. The following table lists the signal correspondences. Refer to the schematic for details

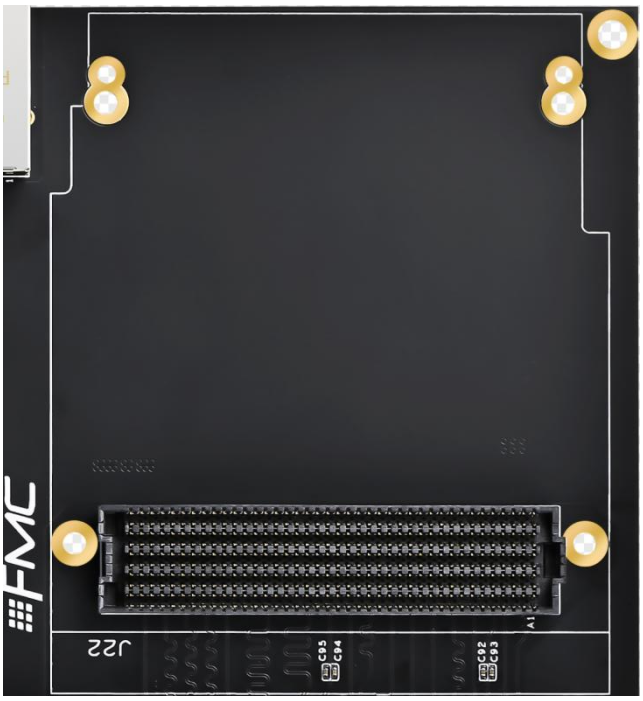
Number	FMC HPC Pin	Pin Name	Pin Position
A2	DP1_M2C_P	MGT_RX_P1_124	BA45
A3	DP1_M2C_N	MGT_RX_N1_124	BA46
A6	DP2_M2C_P	MGT_RX_P2_124	AW45
A7	DP2_M2C_N	MGT_RX_N2_124	AW46
A10	DP3_M2C_P	MGT_RX_P3_124	AV43
A11	DP3_M2C_N	MGT_RX_N3_124	AV44
A14	DP4_M2C_P	MGT_RX_P0_125	AU45
A15	DP4_M2C_N	MGT_RX_N0_125	AU46
A18	DP5_M2C_P	MGT_RX_P1_125	AT43
A19	DP5_M2C_N	MGT_RX_N1_125	AT44
A22	DP1_C2M_P	MGT_TX_P1_124	BD42
A23	DP1_C2M_N	MGT_TX_N1_124	BD43
A26	DP2_C2M_P	MGT_TX_P2_124	BB42
A27	DP2_C2M_N	MGT_TX_N2_124	BB43
A30	DP3_C2M_P	MGT_TX_P3_124	AW40
A31	DP3_C2M_N	MGT_TX_N3_124	AW41
A34	DP4_C2M_P	MGT_TX_P0_125	AU40
A35	DP4_C2M_N	MGT_TX_N0_125	AU41
A38	DP5_C2M_P	MGT_TX_P1_125	AT38
A39	DP5_C2M_N	MGT_TX_N1_125	AT39
B12	DP7_M2C_P	MGT_RX_P3_125	AP43
B13	DP7_M2C_N	MGT_RX_N3_125	AP44
B16	DP6_M2C_P	MGT_RX_P2_125	AR45
B17	DP6_M2C_N	MGT_RX_N2_125	AR46
B20	GBTCLK1_M2C_P	MGT_CLK0_P_125	AV38
B21	GBTCLK1_M2C_N	MGT_CLK0_N_125	AV39
B32	DP7_C2M_P	MGT_TX_P3_125	AP38
B33	DP7_C2M_N	MGT_TX_N3_125	AP39
B36	DP6_C2M_P	MGT_TX_P2_125	AR40
B37	DP6_C2M_N	MGT_TX_N2_125	AR41
C2	DP0_C2M_P	MGT_TX_P0_124	BF42
C3	DP0_C2M_N	MGT_TX_N0_124	BF43
C6	DP0_M2C_P	MGT_RX_P0_124	BC45
C7	DP0_M2C_N	MGT_RX_N0_124	BC46

C10	LA06_P	IO_L2P_65	BE27
C11	LA06_N	IO_L2N_65	BF27
C14	LA10_P	IO_L8P_65	BB26
C15	LA10_N	IO_L8N_65	BB27
C18	LA14_P	IO_L19P_65	AP25
C19	LA14_N	IO_L19N_65	AP26
C22	LA18_P_CC	IO_L12P_GC_65	AW28
C23	LA18_N_CC	IO_L12N_GC_65	AY28
C26	LA27_P	IO_L1P_67	BF14
C27	LA27_N	IO_L1N_67	BF13
C30	SCL	IIC Expansion Chip, Refer to Schematic	
C31	SDA	IIC Expansion Chip, Refer to Schematic	
D4	GBTCLK0_M2C_P	IO_L11P_GC_65	BA40
D5	GBTCLK0_M2C_N	IO_L11N_GC_65	BA41
D8	LA01_P_CC	IO_L4P_65	AY26
D9	LA01_N_CC	IO_L4N_65	AY27
D11	LA05_P	IO_L22P_65	BD26
D12	LA05_N	IO_L22N_65	BE26
D14	LA09_P	IO_L7P_65	AM26
D15	LA09_N	IO_L7N_65	AN26
D17	LA13_P	IO_L14P_GC_65	BA25
D18	LA13_N	IO_L14N_GC_65	BB25
D20	LA17_P_CC	IO_L9P_65	AV27
D21	LA17_N_CC	IO_L9N_65	AV28
D23	LA23_P	IO_L4P_67	BA27
D24	LA23_N	IO_L4N_67	BA28
D26	LA26_P	IO_L11P_GC_64	BD13
D27	LA26_N	IO_L11N_GC_64	BE13
E2	HA01_P_CC	IO_L10P_64	AY22
E3	HA01_N_CC	IO_L10N_64	BA22
E6	HA05_P	IO_L21P_64	BA24
E7	HA05_N	IO_L21N_64	BB24
E9	HA09_P	IO_L3P_64	AN24
E10	HA09_N	IO_L3N_64	AP24
E12	HA13_P	IO_L1P_64	BC24
E13	HA13_N	IO_L1N_64	BD24
E15	HA16_P	IO_L23P_64	BF24
E16	HA16_N	IO_L23N_64	BF23
E18	HA20_P	IO_L4P_66	AL22
E19	HA20_N	IO_L4N_66	AM22
E21	HB03_P	IO_L1P_66	BC19
E22	HB03_N	IO_L1N_66	BD19
E24	HB05_P	IO_L20P_66	BE17
E25	HB05_N	IO_L20N_66	BF17
E27	HB09_P	IO_L15P_66	AN19
E28	HB09_N	IO_L15N_66	AP19
E30	HB13_P	IO_L8P_66	AT18
E31	HB13_N	IO_L8N_66	AU17

E33	HB19_P	IO_L23P_66	AY18
E34	HB19_N	IO_L23N_66	BA18
E36	HB21_P	IO_L12P_GC_64	AL19
E37	HB21_N	IO_L12N_GC_64	AM19
F4	HA00_P_CC	IO_L8P_64	AY23
F5	HA00_N_CC	IO_L8N_64	BA23
F7	HA04_P	IO_L18P_64	BB21
F8	HA04_N	IO_L18N_64	BC21
F10	HA08_P	IO_L2P_64	AT24
F11	HA08_N	IO_L2N_64	AU24
F13	HA12_P	IO_L5P_64	BD23
F14	HA12_N	IO_L5N_64	BE23
F16	HA15_P	IO_L20P_64	BD21
F17	HA15_N	IO_L20N_64	BE21
F19	HA19_P	IO_L2P_66	AN23
F20	HA19_N	IO_L2N_66	AP23
F22	HB02_P	IO_L6P_66	BF19
F23	HB02_N	IO_L6N_66	BF18
F25	HB04_P	IO_L10P_66	BB19
F26	HB04_N	IO_L10N_66	BC18
F28	HB08_P	IO_L16P_66	AV21
F29	HB08_N	IO_L16N_66	AW21
F31	HB12_P	IO_L7P_66	AR17
F32	HB12_N	IO_L7N_66	AT17
F34	HB16_P	IO_L22P_66	AY17
F35	HB16_N	IO_L22N_66	BA17
F37	HB20_P	IO_L13P_GC_67	AL17
F38	HB20_N	IO_L13N_GC_67	AM17
J2	CLK3_M2C_P	IO_L15P_64	AW14
J3	CLK3_M2C_N	IO_L15N_64	AW13
J6	HA03_P	IO_L9P_64	AU22
J7	HA03_N	IO_L9N_64	AV22
J9	HA07_P	IO_L22P_64	BB22
J10	HA07_N	IO_L22N_64	BC22
J12	HA11_P	IO_L17P_64	AL24
J13	HA11_N	IO_L17N_64	AM24
J15	HA14_P	IO_L6P_64	AR23
J16	HA14_N	IO_L6N_64	AT23
J18	HA18_P	IO_L19P_64	BD20
J19	HA18_N	IO_L19N_64	BE20
J21	HA22_P	IO_L3P_66	AN22
J22	HA22_N	IO_L3N_66	AN21
J24	HB01_P	IO_L5P_66	BD18
J25	HB01_N	IO_L5N_66	BE18
J27	HB07_P	IO_L24P_66	BB17
J28	HB07_N	IO_L24N_66	BC17
J30	HB11_P	IO_L18P_66	AL20
J31	HB11_N	IO_L18N_66	AM20

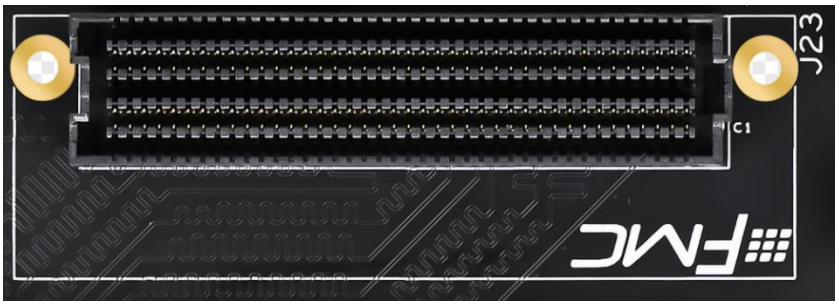
J33	HB15_P	IO_L17P_66	AP20
J34	HB15_N	IO_L17N_66	AR20
J36	HB18_P	IO_L12P_GC_67	AP18
J37	HB18_N	IO_L12N_GC_67	AR18
K4	CLK2_M2C_P	IO_L7P_64	AY13
K5	CLK2_M2C_N	IO_L7N_64	BA13
K7	HA02_P	IO_L13P_GC_64	BA20
K8	HA02_N	IO_L13N_GC_64	BB20
K10	HA06_P	IO_L4P_64	AV23
K11	HA06_N	IO_L4N_64	AW23
K13	HA10_P	IO_L14P_GC_64	BE22
K14	HA10_N	IO_L14N_GC_64	BF22
K16	HA17_P_CC	IO_L16P_64	AV24
K17	HA17_N_CC	IO_L16N_64	AW24
K19	HA21_P	IO_L24P_64	AR22
K20	HA21_N	IO_L24N_64	AT22
K22	HA23_P	IO_L13P_GC_66	AL21
K23	HA23_N	IO_L13N_GC_66	AM21
K25	HB00_P_CC	IO_L14P_GC_66	AT19
K26	HB00_N_CC	IO_L14N_GC_66	AU19
K28	HB06_P_CC	IO_L9P_66	AT20
K29	HB06_N_CC	IO_L9N_66	AU20
K31	HB10_P	IO_L19P_66	AW20
K32	HB10_N	IO_L19N_66	AY20
K34	HB14_P	IO_L12P_GC_66	AN18
K35	HB14_N	IO_L12N_GC_66	AN17
K37	HB17_P_CC	IO_L11P_GC_67	AV19
K38	HB17_N_CC	IO_L11N_GC_67	AW19
G2	CLK1_M2C_P	IO_L13P_GC_65	BA15
G3	CLK1_M2C_N	IO_L13N_GC_65	BA14
G6	LA00_P_CC	IO_L1P_65	AV26
G7	LA00_N_CC	IO_L1N_65	AW26
G9	LA03_P	IO_L5P_65	BF28
G10	LA03_N	IO_L5N_65	BF29
G12	LA08_P	IO_L10P_65	BE25
G13	LA08_N	IO_L10N_65	BF25
G15	LA12_P	IO_L20P_65	AW25
G16	LA12_N	IO_L20N_65	AY25
G18	LA16_P	IO_L23P_65	AN28
G19	LA16_N	IO_L23N_65	AP28
G21	LA20_P	IO_L21P_65	AM27
G22	LA20_N	IO_L21N_65	AN27
G24	LA22_P	IO_L19P_67	AL25
G25	LA22_N	IO_L19N_67	AM25
G27	LA25_P	IO_L22P_67	AR16
G28	LA25_N	IO_L22N_67	AR15
G30	LA29_P	IO_L15P_67	AP13
G31	LA29_N	IO_L15N_67	AR13

G33	LA31_P	IO_L23P_67	AU13
G34	LA31_N	IO_L23N_67	AV13
G36	LA33_P	IO_L11P_GC_66	AL15
G37	LA33_N	IO_L11N_GC_66	AM15
H4	CLK0_M2C_P	IO_L6P_65	AV18
H5	CLK0_M2C_N	IO_L6N_65	AW18
H7	LA02_P	IO_L3P_65	BC26
H8	LA02_N	IO_L3N_65	BC27
H10	LA04_P	IO_L18P_65	BD28
H11	LA04_N	IO_L18N_65	BE28
H13	LA07_P	IO_L15P_65	AR28
H14	LA07_N	IO_L15N_65	AT28
H16	LA11_P	IO_L17P_65	AU26
H17	LA11_N	IO_L17N_65	AU27
H19	LA15_P	IO_L24P_65	AR27
H20	LA15_N	IO_L24N_65	AT27
H22	LA19_P	IO_L16P_65	AL27
H23	LA19_N	IO_L16N_65	AL28
H25	LA21_P	IO_L16P_67	AR25
H26	LA21_N	IO_L16N_67	AT25
H28	LA24_P	IO_L18P_67	AU14
H29	LA24_N	IO_L18N_67	AV14
H31	LA28_P	IO_L3P_67	AU16
H32	LA28_N	IO_L3N_67	AV16
H34	LA30_P	IO_L9P_67	BD16
H35	LA30_N	IO_L9N_67	BE16
H37	LA32_P	IO_L3P_64	AY16
H38	LA32_N	IO_L3N_64	AY15



Number	FMC LPC 1 Pin	Pin Name	Pin Position
C2	DP0_C2M_P	MGT_TX_P3_133	A42
C3	DP0_C2M_N	MGT_TX_N3_133	A43
C6	DP0_M2C_P	MGT_RX_P3_133	D45
C7	DP0_M2C_N	MGT_RX_N3_133	D46
C10	LA06_P	IO_L18P_74	E25
C11	LA06_N	IO_L18N_74	D25
C14	LA10_P	IO_L24P_74	B25
C15	LA10_N	IO_L24N_74	A25
C18	LA14_P	IO_L22P_74	A23
C19	LA14_N	IO_L22N_74	A22
C22	LA18_P_CC	IO_L12P_GC_74	J24
C23	LA18_N_CC	IO_L12N_GC_74	H24
C26	LA27_P	IO_L21P_73	C21
C27	LA27_N	IO_L21N_73	B21
C30	SCL	IIC Expansion Chip, Refer to Schematic	
C31	SDA	IIC Expansion Chip, Refer to Schematic	
D4	GBTCLK0_M2C_P	MGT_CLK0_P_133	L36
D5	GBTCLK0_M2C_N	MGT_CLK0_N_133	L37
D8	LA01_P_CC	IO_L13P_GC_74	G25
D9	LA01_N_CC	IO_L13N_GC_74	G24
D11	LA05_P	IO_L21P_74	C26
D12	LA05_N	IO_L21N_74	B26
D14	LA09_P	IO_L23P_74	B24
D15	LA09_N	IO_L23N_74	A24
D17	LA13_P	IO_L19P_74	C22
D18	LA13_N	IO_L19N_74	B22
D20	LA17_P_CC	IO_L11P_GC_74	J23
D21	LA17_N_CC	IO_L11N_GC_74	H23
D23	LA23_P	IO_L1P_74	R21
D24	LA23_N	IO_L1N_74	P21
D26	LA26_P	IO_L19P_73	D19
D27	LA26_N	IO_L19N_73	C19
G2	CLK1_M2C_P	IO_L14P_GC_74	F24
G3	CLK1_M2C_N	IO_L14N_GC_74	F23
G6	LA00_P_CC	IO_L14P_GC_73	G20
G7	LA00_N_CC	IO_L14N_GC_73	G19
G9	LA03_P	IO_L6P_74	R25
G10	LA03_N	IO_L6N_74	P25
G12	LA08_P	IO_L4P_74	P24
G13	LA08_N	IO_L4N_74	N24
G15	LA12_P	IO_L5P_74	M25
G16	LA12_N	IO_L5N_74	M24
G18	LA16_P	IO_L3P_74	P23
G19	LA16_N	IO_L3N_74	N23
G21	LA20_P	IO_L2P_74	N22
G22	LA20_N	IO_L2N_74	M22

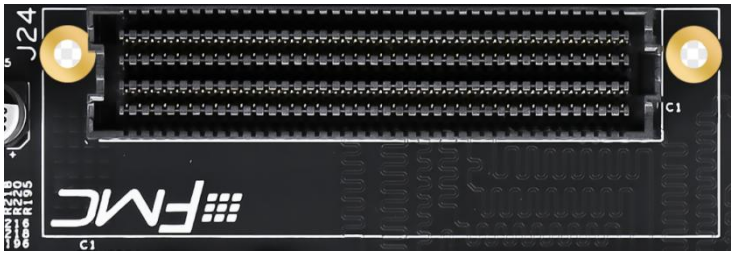
G24	LA22_P	IO_L8P_74	L22
G25	LA22_N	IO_L8N_74	K22
G27	LA25_P	IO_L17P_73	E21
G28	LA25_N	IO_L17N_73	E20
G30	LA29_P	IO_L10P_73	J21
G31	LA29_N	IO_L10N_73	H21
G33	LA31_P	IO_L6P_73	N21
G34	LA31_N	IO_L6N_73	M21
G36	LA33_P	IO_L24P_73	B20
G37	LA33_N	IO_L24N_73	A20
H4	CLK0_M2C_P	IO_L13P_GC_73	H19
H5	CLK0_M2C_N	IO_L13N_GC_73	H18
H7	LA02_P	IO_L10P_74	K25
H8	LA02_N	IO_L10N_74	J25
H10	LA04_P	IO_L7P_74	L25
H11	LA04_N	IO_L7N_74	L24
H13	LA07_P	IO_L15P_74	G22
H14	LA07_N	IO_L15N_74	F22
H16	LA11_P	IO_L16P_74	E23
H17	LA11_N	IO_L16N_74	E22
H19	LA15_P	IO_L17P_74	D24
H20	LA15_N	IO_L17N_74	D23
H22	LA19_P	IO_L20P_74	C24
H23	LA19_N	IO_L20N_74	C23
H25	LA21_P	IO_L9P_74	L23
H26	LA21_N	IO_L9N_74	K23
H28	LA24_P	IO_L20P_73	D21
H29	LA24_N	IO_L20N_73	D20
H31	LA28_P	IO_L15P_73	F20
H32	LA28_N	IO_L15N_73	F19
H34	LA30_P	IO_L5P_73	R20
H35	LA30_N	IO_L5N_73	P20
H37	LA32_P	IO_L23P_73	B19
H38	LA32_N	IO_L23N_73	A19



Number	FMC LPC 2 Pin	Pin Name	Pin Position
C2	DP0_C2M_P	MGT_TX_P2_233	C9
C3	DP0_C2M_N	MGT_TX_N2_233	C8

C6	DP0_M2C_P	MGT_RX_P2_233	C4
C7	DP0_M2C_N	MGT_RX_N2_233	C3
C10	LA06_P	IO_L24P_72	B17
C11	LA06_N	IO_L24N_72	A17
C14	LA10_P	IO_L21P_72	A14
C15	LA10_N	IO_L21N_72	A13
C18	LA14_P	IO_L19P_72	D13
C19	LA14_N	IO_L19N_72	C13
C22	LA18_P_CC	IO_L11P_GC_72	J14
C23	LA18_N_CC	IO_L11N_GC_72	H14
C26	LA27_P	IO_L4P_73	P19
C27	LA27_N	IO_L4N_73	N19
C30	SCL	IIC Expansion Chip, Refer to Schematic	
C31	SDA	IIC Expansion Chip, Refer to Schematic	
D4	GBTCLK0_M2C_P	MGT_CLK0_P_233	D11
D5	GBTCLK0_M2C_N	MGT_CLK0_N_233	D10
D8	LA01_P_CC	IO_L13P_GC_72	G14
D9	LA01_N_CC	IO_L13N_GC_72	F14
D11	LA05_P	IO_L23P_72	C16
D12	LA05_N	IO_L23N_72	B16
D14	LA09_P	IO_L22P_72	B15
D15	LA09_N	IO_L22N_72	A15
D17	LA13_P	IO_L20P_72	C14
D18	LA13_N	IO_L20N_72	B14
D20	LA17_P_CC	IO_L12P_GC_72	J16
D21	LA17_N_CC	IO_L12N_GC_72	J15
D23	LA23_P	IO_L5P_72	M14
D24	LA23_N	IO_L5N_72	L14
D26	LA26_P	IO_L2P_73	P18
D27	LA26_N	IO_L2N_73	N18
G2	CLK1_M2C_P	IO_L12P_GC_73	J20
G3	CLK1_M2C_N	IO_L12N_GC_73	J19
G6	LA00_P_CC	IO_L14P_GC_72	G15
G7	LA00_N_CC	IO_L14N_GC_72	F15
G9	LA03_P	IO_L18P_72	E16
G10	LA03_N	IO_L18N_72	D16
G12	LA08_P	IO_L10P_72	H17
G13	LA08_N	IO_L10N_72	H16
G15	LA12_P	IO_L3P_72	R15
G16	LA12_N	IO_L3N_72	P15
G18	LA16_P	IO_L9P_72	J13
G19	LA16_N	IO_L9N_72	H13
G21	LA20_P	IO_L8P_72	K16
G22	LA20_N	IO_L8N_72	K15
G24	LA22_P	IO_L7P_72	L13
G25	LA22_N	IO_L7N_72	K13
G27	LA25_P	IO_L9P_73	L20
G28	LA25_N	IO_L9N_73	K20

G30	LA29_P	IO_L8P_73	L19
G31	LA29_N	IO_L8N_73	L18
G33	LA31_P	IO_L7P_73	L17
G34	LA31_N	IO_L7N_73	K17
G36	LA33_P	IO_L16P_73	E18
G37	LA33_N	IO_L16N_73	E17
H4	CLK0_M2C_P	IO_L11P_GC_73	K18
H5	CLK0_M2C_N	IO_L11N_GC_73	J18
H7	LA02_P	IO_L16P_72	G17
H8	LA02_N	IO_L16N_72	G16
H10	LA04_P	IO_L17P_72	E15
H11	LA04_N	IO_L17N_72	D15
H13	LA07_P	IO_L4P_72	R16
H14	LA07_N	IO_L4N_72	P16
H16	LA11_P	IO_L15P_72	F13
H17	LA11_N	IO_L15N_72	E13
H19	LA15_P	IO_L6P_72	N16
H20	LA15_N	IO_L6N_72	M16
H22	LA19_P	IO_L2P_72	P14
H23	LA19_N	IO_L2N_72	N14
H25	LA21_P	IO_L1P_72	P13
H26	LA21_N	IO_L1N_72	N13
H28	LA24_P	IO_L3P_73	M20
H29	LA24_N	IO_L3N_73	M19
H31	LA28_P	IO_L1P_73	N17
H32	LA28_N	IO_L1N_73	M17
H34	LA30_P	IO_L18P_73	F18
H35	LA30_N	IO_L18N_73	F17
H37	LA32_P	IO_L22P_73	D18
H38	LA32_N	IO_L22N_73	C18

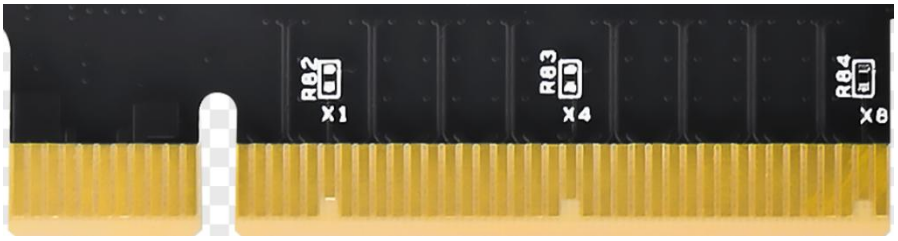


Part 4.14: PCIE 3.0 Interface

PCIE 3.0 Interface is designed on the FPGA carrier board, is x 8 interface, The following table lists the PCIE interface correspondences.

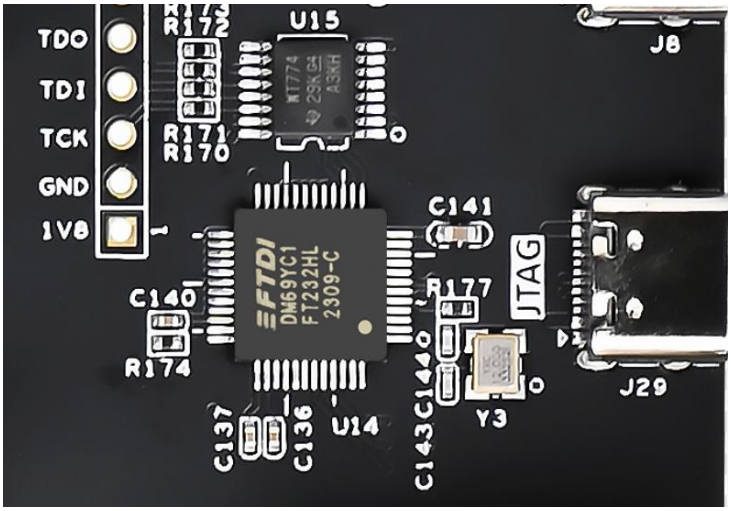
PCIE3.0	Pin Name	Pin Position
PERST_N	IO_2N_68	BF8
REF_CLK_P	MGT_110_CLK_P0	AW9
REF_CLK_N	MGT_110_CLK_N0	AW8

PER0_P	MGT_TX_P0_224	BF5
PER0_N	MGT_TX_N0_224	BF4
PER1_P	MGT_TX_P1_224	BD5
PER1_N	MGT_TX_N1_224	BD4
PER2_P	MGT_TX_P2_224	BB5
PER2_N	MGT_TX_N2_224	BB4
PER3_P	MGT_TX_P3_224	AV7
PER3_N	MGT_TX_N3_224	AV6
PER4_P	MGT_TX_P0_225	AU9
PER4_N	MGT_TX_N0_225	AU8
PER5_P	MGT_TX_P1_225	AT7
PER5_N	MGT_TX_N1_225	AT6
PER6_P	MGT_TX_P2_225	AR9
PER6_N	MGT_TX_N2_225	AR8
PER7_P	MGT_TX_P3_225	AP7
PER7_N	MGT_TX_N3_225	AP6
PET0_P	MGT_RX_P0_224	BC2
PET0_N	MGT_RX_N0_224	BC1
PET1_P	MGT_RX_P1_224	BA2
PET1_N	MGT_RX_N1_224	BA1
PET2_P	MGT_RX_P2_224	AW4
PET2_N	MGT_RX_N2_224	AW3
PET3_P	MGT_RX_P3_224	AV2
PET3_N	MGT_RX_N3_224	AV1
PET4_P	MGT_RX_P0_225	AU4
PET4_N	MGT_RX_N0_225	AU3
PET5_P	MGT_RX_P1_225	AT2
PET5_N	MGT_RX_N1_225	AT1
PET6_P	MGT_RX_P2_225	AR4
PET6_N	MGT_RX_N2_225	AR3
PET7_P	MGT_RX_P3_225	AP2
PET7_N	MGT_RX_N3_225	AP1



Part 4.15: USB to JTAG Programmer

USB to **JTAG** Programmer onboard is designed on the FPGA carrier board. After installing the **Vivado** software, use a **USB** cable to connect the USB port corresponding to JTAG. You can realize debugging and downloading, which is very convenient. The following is the location of the interface on the FPGA development board.


TDO
TDI
TCK
GND
1V8
R172
U15
J8
R171
R170
C141
C140
R174
R177
JTAG
FTDI
DM69YC1
FT232HL
2309-C
C144
Y3
J29
C137
C136
U14
C143