AMD Kintex UltraScale+

CRKU3PB/CRKU5PB

User Manual



Version Records:

Data	Version	Description
2024.05.25	V1.0	initial version

This tutorial will continue to revise, optimize and increase based on the actual Experience, that is to provide you with more and better Demos.

If you find some errors or any suggestion, contact with us.

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Part 1: AMD Kintex™ UltraScale+™

AMD **Kintex™ UltraScale+™** devices provide the best price/performance/watt balance in a FinFET node, delivering a cost-effective solution for applications that require high-end capabilities including 33 Gb/s transceivers and 100G connectivity cores. Our mid-range family is ideal for both packet processing and DSP-intensive functions and is well suited for applications such as wireless MIMO technology, Nx100G wired networking, and data center networking and storage acceleration.

HIGHLIGHTS

Programmable System Integration

- Up to 1.2M system logic cells
- UltraRAM for on-chip memory integration
- Integrated 100G Ethernet MAC with KR4 RS-FEC, PCIe® Gen4, and 150G Interlaken core

Increased System Performance

- 6.3 TeraMACs of DSP compute performance
- Over 2X system-level performance per watt over Kintex 7 FPGAs
- 16G and 28G backplane-capable transceivers
- 2666 Mb/s DDR4 in the mid-speed grade

BOM Cost Reduction

- 12.5 Gb/s transceivers in slowest speed grade
- VCXO and fractional PLL integration reduces clocking component cost

Total Power Reduction

- Up to 60% lower power vs. 7 series FPGAs
- Voltage scaling options for performance and power
- Tighter logic cell packing for dynamic power reduction

Accelerated Design Productivity

- Co-optimized with Vivado™ Design Suite for rapid design closure
- SmartConnect technology for intelligent IP integration

Kintex UltraScale+ device resources are as follows

XCKU3P | XCKU5P | XCKU9P | XCKU11P | XCKU13P | XCKU15P | XCKU19P

COMPARE | Reset

	XCKU3P	XCKU5P	XCKU9P	XCKU11P	XCKU13P	XCKU
System Logic Cells (K)	356	475	600	653	747	1,143
CLB LUTs (K)	163	217	274	299	341	523
DSP Slices	1,368	1,824	2,520	2,928	3,528	1,968
Memory (Mb)	26.2	34.9	32.1	43.6	57.7	70.6
GTH 16.3 Gb/s Transceivers	0	0	28	32	28	44
GTY 32.75 Gb/s Transceivers	16	16	0	20	0	32
I/O Pins	304	304	304	512	304	668

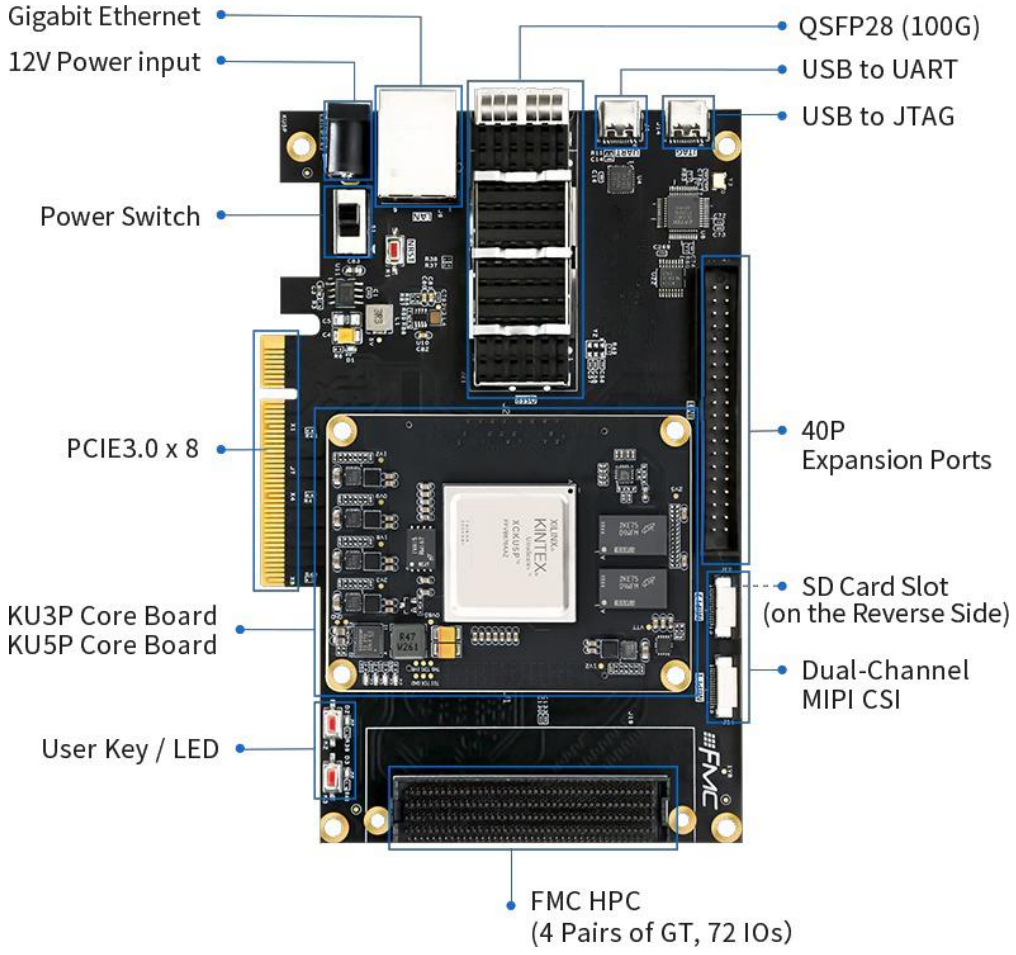
Part 2: CRKU3PB CRKU5PB FPGA Board Overview

Part 2.1: Board Introduction

The Kintex UltraScale+ Series FPGA development board adopts the mode of "Core board + Carrier board". The core board is snapped to the carrier board with two 0.635mm pitch 240P high-speed connectors for more flexible use. It can be used for learning or for project development. There are two versions: CRKU3PB and CRKU5PB, respectively using XCKU3P-2FFVB676I andXCKU5P-2FFVB676I chips from XILINX as the main controller.

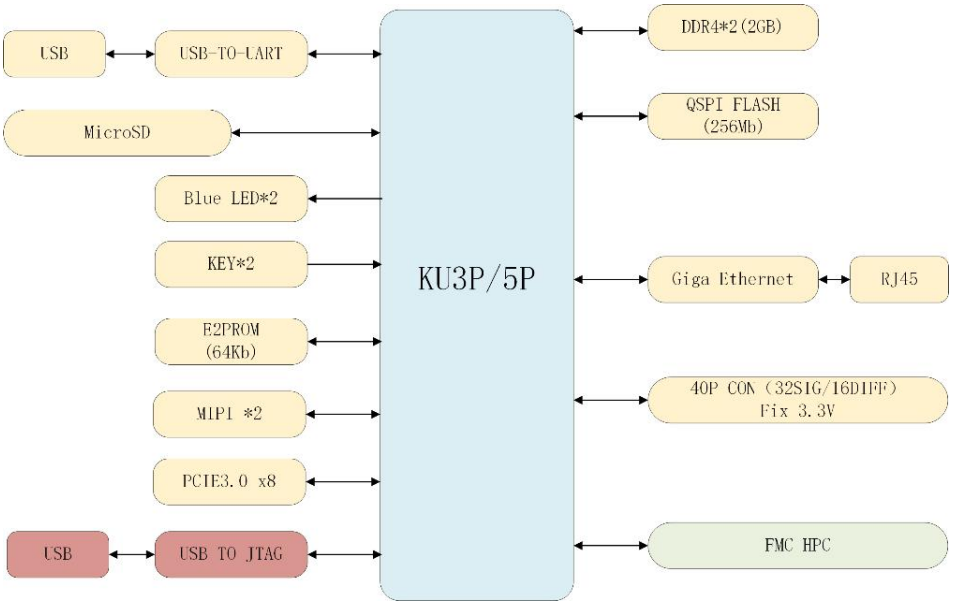
In addition, the FPGA development board integrates a wealth of peripheral resources, provides detailed development routines, and accelerates user learning or project advancement. In addition, the development board also integrates a JTAG debugger, so that a USB cable and a 12V power cable can make the development board work and be more convenient to use.

The Form Factors of the FPGA development board is 148mm x 100mm, and a fixing hole is placed at each of the four corners of the board to install the support column or fix the board, and the hole diameter is 3.5mm. The fpga board as below



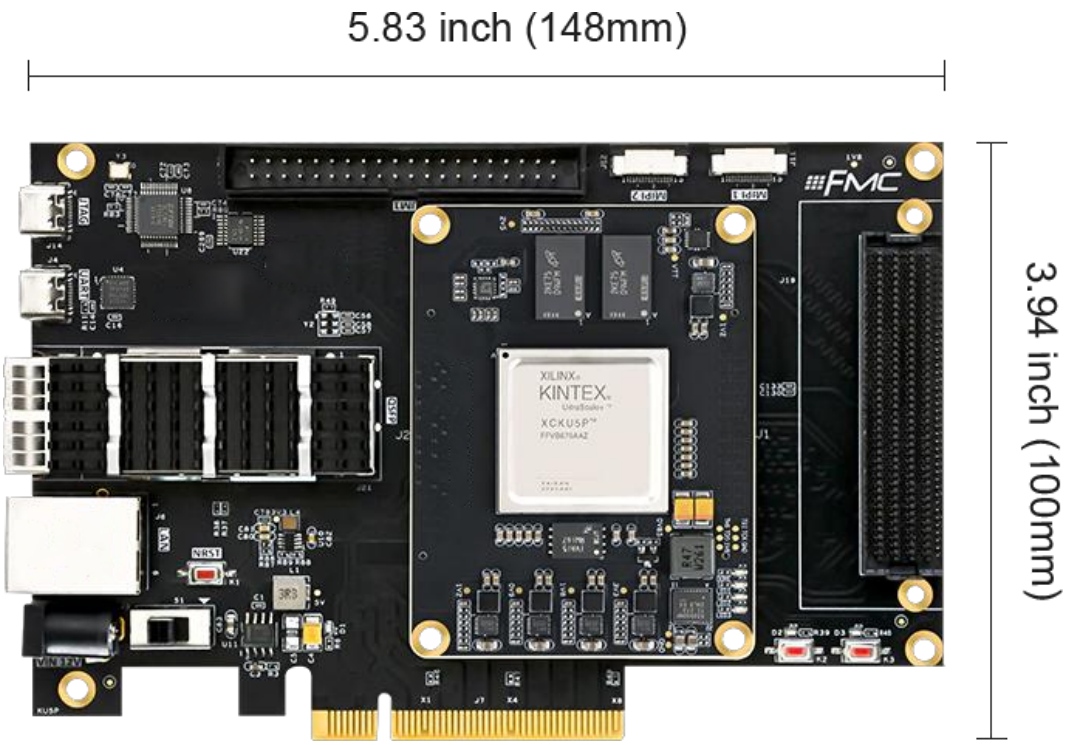
Part 2.2: Product Function Block Diagram

In this section, we will show the configuration details of the product in detail through the product block diagram, as shown below.



Part 2.3: Form Factors

The Form Factors of the FPGA development board is 148mm x 100mm (5.83inch x 3.94inch)



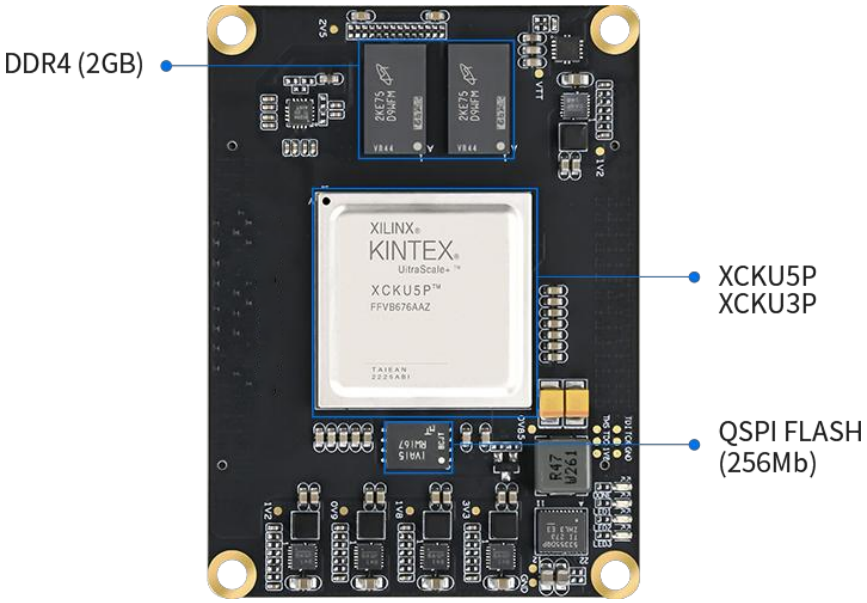
The heat dissipation is made up of customized fans, heat sinks. and acrylic protective plate, for the convenience of display, and not installed on the FPGA development board. The form factors of the heat dissipation as below:

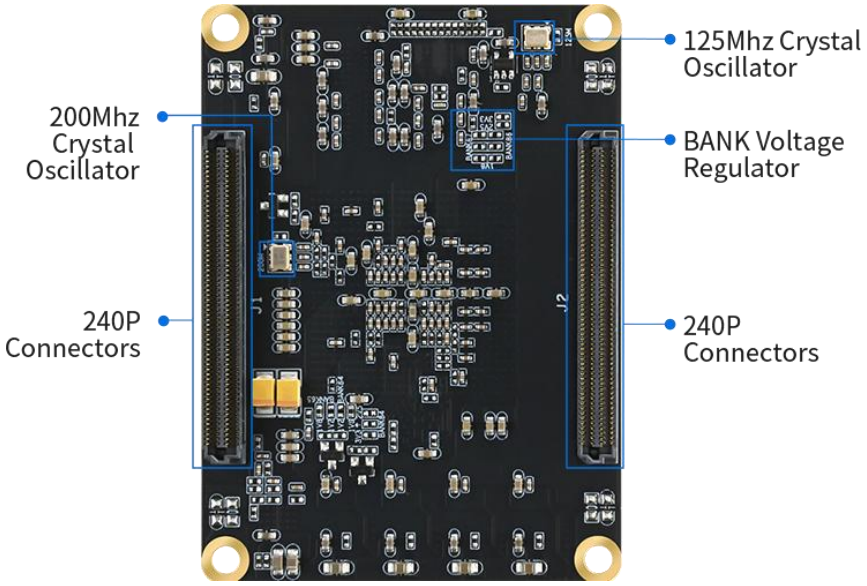


Part 3: CRKU3PC and CRKU5PC CoreBoard Overview

Part 3.1: SOM Introduction

FPGA development board using the core board snap-on the carrier board, the FPGA development board model depends on the use of the core board model. Core board provides CRKU3PC and CRKU5PC two models, the two core board interface is fully compatible, replacement of the core board can be realized by replacing the model of the development board, in this section will describes the two core boards in detail.

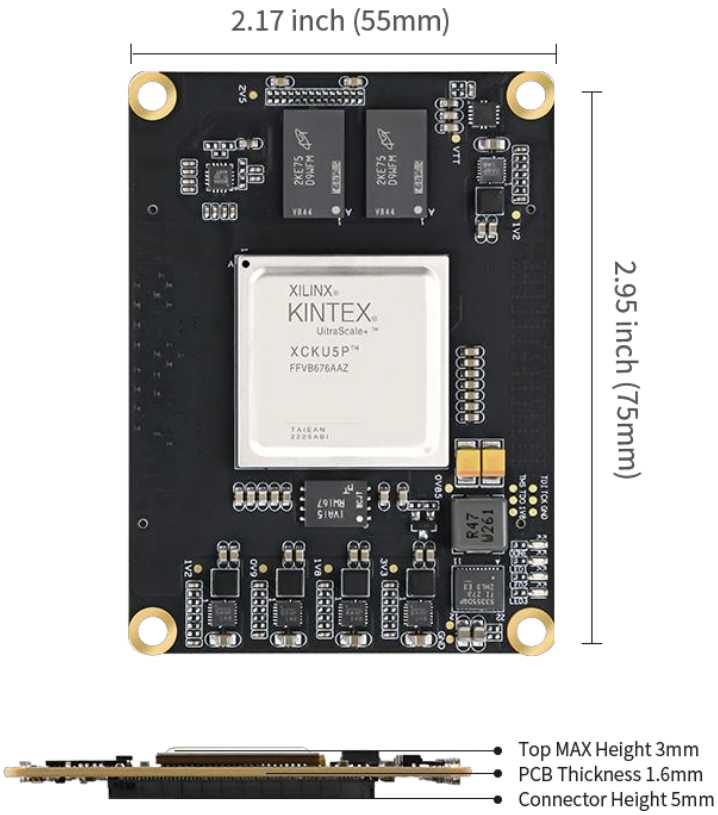




Part 3.2: SOM Specification

The following table lists all the on-board resources of the core board, and compare the differences between the two core boards in detail.

FPGA SOM	KU3P	KU5P
FPGA Chip	XCKU3P-2FFVB676I	XCKU5P-2FFVB676I
Speed Grade	2	
Chip Level	Industrial Grade（-40°C~+85°C）	
Logic Cells	356k	475k
Lookup Tables (LUTs)	163k	217k
Flip-Flops	325k	434k
DSP Slices	1368	1824
BLOCK RAM	12.7Mb	16.9Mb
DDR4	2GB/32bit Width	
QSPI FLASH	256Mb, to Store Startup Files and User Files	
Start-up Mode	JTAG/QSPI, The Default Boot Mode is QSPI	
User LED	3	
Number of GTY	16 Pairs of TX/RX	
Number of IO	168 single-ended/84 differential HP: 96 IOs Levels fixed at 1.2V/ 1.8V (Default 1.8V) HD: 72 IOs Levels 1.8/2.5/3.3V Adjustable (Default 3.3V)	
Voltage/ Current	5V/3A	
Crystal Oscillator	Differential Single-ended Crystal 200MHz for FPGA Differential Single-ended Crystal 125MHz for the GT Transceiver Reference Clock	
Technology	Black Matte. Immersion Gold Process	
Core Board Form Factors	2.95 inch x 2.17 inch (75mm x 55mm)	

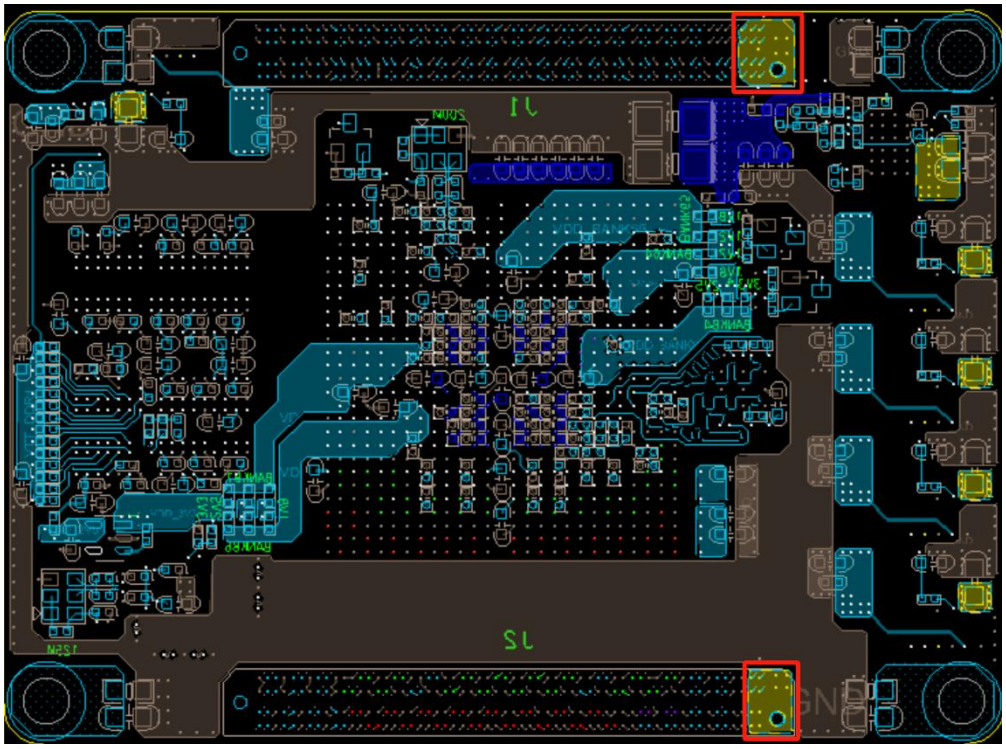


Part 3.3: Power Connection

The power supply voltage range of the core board is 5V. There are power input pins on the two corners of the core board. The power pins have been connected inside the module. Considering that the chip consumes a large amount of current, both corners of the power supply need to be connected to an external power supply to ensure that the power supply current is sufficient.

The power connection needs to be connected with copper and enough through holes are made to ensure the power flow capacity. All GND signals on the core board need to be connected to the carrier board, and each GND is connected to the carrier board through two vias. The limit current of the core board power supply is 5V/3A, so the external power supply needs to consider the limit current to ensure the stable operation of the core board.

Power supply output voltage to the module needs to be stable, and need to consider the power surge, the core board power input port needs to be a few larger capacitors **(220uF/10V)**, if the cost allows, you can add a level of DC2DC chip, to ensure that the power supply is stable.

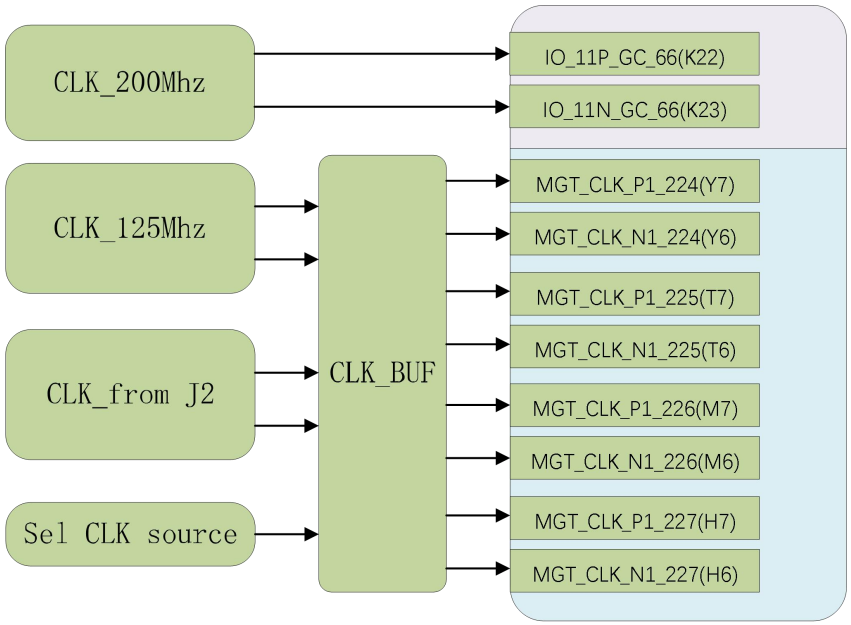


Part 3.4: Clock

The core board provides multiple differential clocks with frequencies of 200M/125M to meet various application requirements. In addition, the 125M clock is added with a clock buffer, which can realize the switching between on-board clock and external clock input.

When the clock selection signal is not grounded, the clock source is the differential crystal. When the clock selection signal is grounded, the clock source is the external input of the connector,

the following diagram lists the clock connections and pin locations, more details refer to the core board schematic.



Part 3.5: Core Board Reset

Considering the maximum retention of IO ports leading to the carrier board, the core board does not add a reset key, an one reset key is designed on the FPGA Carrier board. Because the master chip is a pure FPGA, any IO interface can be used as a logical reset interface, and the user can also define his own reset interface.

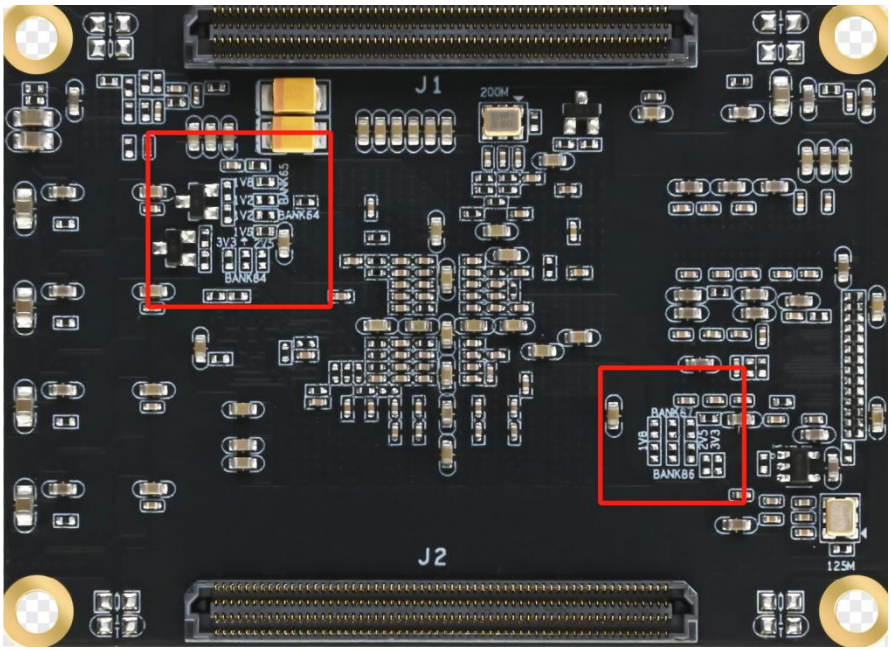
Part 3.6: Boot Mode Selection

The boot mode of the main chip are JTAG, QSPI Flash, the default configuration is QSPI Flash start, but JTAG mode priority is higher than QSPI Flash, so when the user connected to the JTAG interface, the chip priority from JTAG start, do not have to do boot mode switching. The capacity of QSPI Flash on the core board is 256Mb, for more detailed refer to the schematic..

Part 3.7: BANK Interface Level Selection

The BANK64/65 on the core board are HP BANK, the interface level is configured as 1.2/1.8V, the default level is 1.8V. BANK84/86/87 are HD BANK, the interface level can be adjusted 1.8/2.5/3.3V, the default level is 3.3V, and the voltage can be adjusted by resistance welding through the instructions provided on the carrier board, and the default level is 1.8V.

The corresponding resistor labeling locations are shown below.



Part 3.8: DDR4

Two group of DDR4 are designed on the core board, each group of four industrial-grade DDR4 chips, a single capacity of 2GB, four total capacity of 8GB, two group DDR4 total capacity of 16GB, pin assignment as table below, more details refer to the core board schematic

The main chip configuration of two DDR4, single capacity 1GB, two total capacity of 2GB, DDR4 pin assignment as table below, , more details refer to the core board schematic

DDR4 Pin	Pin Name	Pin Position
DDR4_DQ0	IO_L21P_T3L_N4_AD8P_67	C23
DDR4_DQ1	IO_L24N_T3U_N11_67	B22
DDR4_DQ2	IO_L23P_T3U_N8_67	A24
DDR4_DQ3	IO_L24P_T3U_N10_67	C22
DDR4_DQ4	IO_L21N_T3L_N5_AD8N_67	B24
DDR4_DQ5	IO_L20N_T3L_N3_AD1N_67	D21
DDR4_DQ6	IO_L23N_T3U_N9_67	A25
DDR4_DQ7	IO_L20P_T3L_N2_AD1P_67	E21
DDR4_DM0	IO_L19P_T3L_N0_DBC_AD9P_67	A22
DDR4_DQS_P0	IO_L22P_T3U_N6_DBC_AD0P_67	C21
DDR4_DQS_N0	IO_L22N_T3U_N7_DBC_AD0N_67	B21
DDR4_DQ8	IO_L18P_T2U_N10_AD2P_67	A19
DDR4_DQ9	IO_L15N_T2L_N5_AD11N_67	B17
DDR4_DQ10	IO_L18N_T2U_N11_AD2N_67	A20
DDR4_DQ11	IO_L15P_T2L_N4_AD11P_67	C17
DDR4_DQ12	IO_L14N_T2L_N3_GC_67	B20

DDR4_DQ13	IO_L17P_T2U_N8_AD10P_67	B15
DDR4_DQ14	IO_L14P_T2L_N2_GC_67	B19
DDR4_DQ15	IO_L17N_T2U_N9_AD10N_67	A15
DDR4_DM1	IO_L13P_T2L_N0_GC_QBC_67	C18
DDR4_DQS_P1	IO_L16P_T2U_N6_QBC_AD3P_67	A17
DDR4_DQS_N1	IO_L16N_T2U_N7_QBC_AD3N_67	A18
DDR4_DQ16	IO_L12P_T1U_N10_GC_67	D19
DDR4_DQ17	IO_L8N_T1L_N3_AD5N_67	F19
DDR4_DQ18	IO_L12N_T1U_N11_GC_67	D20
DDR4_DQ19	IO_L9P_T1L_N4_AD12P_67	G20
DDR4_DQ20	IO_L9N_T1L_N5_AD12N_67	G21
DDR4_DQ21	IO_L8P_T1L_N2_AD5P_67	F18
DDR4_DQ22	IO_L11N_T1U_N9_GC_67	D18
DDR4_DQ23	IO_L11P_T1U_N8_GC_67	E18
DDR4_DM2	IO_L7P_T1L_N0_QBC_AD13P_67	H18
DDR4_DQS_P2	IO_L10P_T1U_N6_QBC_AD4P_67	F20
DDR4_DQS_N2	IO_L10N_T1U_N7_QBC_AD4N_67	E20
DDR4_DQ24	IO_L3P_T0L_N4_AD15P_67	E15
DDR4_DQ25	IO_L5N_T0U_N9_AD14N_67	G16
DDR4_DQ26	IO_L3N_T0L_N5_AD15N_67	D15
DDR4_DQ27	IO_L2N_T0L_N3_67	G17
DDR4_DQ28	IO_L6P_T0U_N10_AD6P_67	D16
DDR4_DQ29	IO_L2P_T0L_N2_67	H17
DDR4_DQ30	IO_L6N_T0U_N11_AD6N_67	C16
DDR4_DQ31	IO_L5P_T0U_N8_AD14P_67	H16
DDR4_DM3	IO_L1P_T0L_N0_DBC_67	G15
DDR4_DQS_P3	IO_L4P_T0U_N6_DBC_AD7P_67	E16
DDR4_DQS_N3	IO_L4N_T0U_N7_DBC_AD7N_67	E17
DDR4_A0	IO_L20P_T3L_N2_AD1P_66	F23
DDR4_A1	IO_L21N_T3L_N5_AD8N_66	D25
DDR4_A2	IO_L22P_T3U_N6_DBC_AD0P_66	D23
DDR4_A3	IO_L24N_T3U_N11_66	B26
DDR4_A4	IO_L20N_T3L_N3_AD1N_66	E23
DDR4_A5	IO_L23N_T3U_N9_66	C26
DDR4_A6	IO_L16P_T2U_N6_QBC_AD3P_66	F24
DDR4_A7	IO_L23P_T3U_N8_66	D26
DDR4_A8	IO_L17P_T2U_N8_AD10P_66	H26
DDR4_A9	IO_L19P_T3L_N0_DBC_AD9P_66	E25
DDR4_A10	IO_L22N_T3U_N7_DBC_AD0N_66	C24
DDR4_A11	IO_T3U_N12_66	F22
DDR4_A12	IO_L24P_T3U_N10_66	B25
DDR4_A13	IO_L19N_T3L_N1_DBC_AD9N_66	E26

DDR4_A14	IO_L21P_T3L_N4_AD8P_66	D24
DDR4_A15	IO_L12P_T1U_N10_GC_66	J23
DDR4_A16	IO_T2U_N12_66	G22
DDR4_A17	IO_L16N_T2U_N7_QBC_AD3N_66	F25
DDR4_BA0	IO_L15P_T2L_N4_AD11P_66	J25
DDR4_BA1	IO_L18P_T2U_N10_AD2P_66	H21
DDR4_BG0	IO_L17N_T2U_N9_AD10N_66	G26
DDR4_nCS	IO_L14P_T2L_N2_GC_66	H23
DDR4_ODT	IO_T1U_N12_66	M24
DDR4_nRESET	IO_L10N_T1U_N7_QBC_AD4N_66	L25
DDR4_CLK_P	IO_L13P_T2L_N0_GC_QBC_66	G24
DDR4_CLK_N	IO_L13N_T2L_N1_GC_QBC_66	G25
DDR4_CKE	IO_L14N_T2L_N3_GC_66	H24
DDR4_nACT	IO_L10P_T1U_N6_QBC_AD4P_66	L24
DDR4_nALERT	IO_L18N_T2U_N11_AD2N_66	H22
DDR4_PARITY	IO_L15N_T2L_N5_AD11N_66	J26

Part 3.9: Core Board Signal and Equal Length

The signals leading out of the core board to the connectors are strictly equalized, refer to the excel of "KU3P-KU5P Core Board Pins and Equal Length", which detailed list of signal names and signal alignment lengths.

Part 3.10: Core Board Package Library

In order to facilitate the user to quickly use the core board, we provide the corresponding package library, the relative position of the connector and the core board frame silkscreen have been placed, you can directly call to use it.

The schematic package provides two versions of AD/ORCAD, and the PCB package provides two versions of AD/Allegro, which are stored in the corresponding folder.

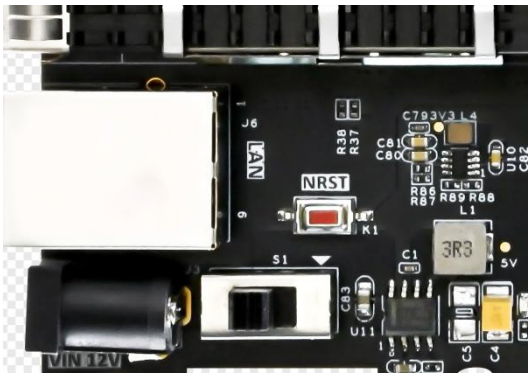
Part 3.11: Core Board Connectors

The core board is connected to the carrier board via four 0.635mm/240P gold-plated high-speed connectors on the bottom. The connector model used on the carrier board is **ADM6-60-01.5-L-4-2-A-TR.**

Part 4: Carrier Board Overview

Part 4.1: Power Supply

The FPGA development board is powered by a 12V/3A adapter or by PCIE.The two power supplies can be switched via the S1 switch. After the power supply is connected, it is converted into 3.3V, 1.8V and other multi-channel voltages through DCDC for use by the devices on the board. the detailed circuit of the power supply part can refer to the corresponding schematic of the FPGA development board



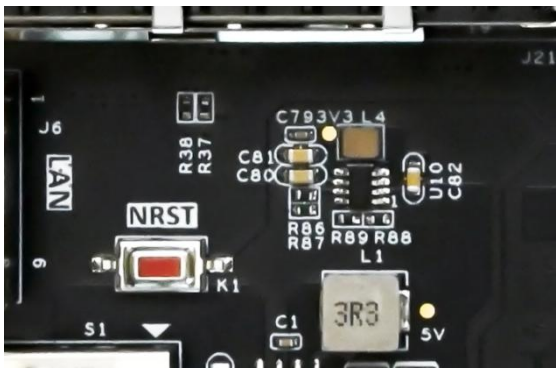
Part 4.2: System Clock

The clock circuit is mainly on the core board, you can refer to the core board clock section for reference

Part 4.3: System Reset

One Reset key is reserved on the FPGA carrier board. The key is high by default and low when pressed.

The reset pin is connected to the IO_4N_84 （AD14) pin of the BANK68 with a level of 3.3 V. For detailed circuitry of the reset part, please refer to the schematic of the FPGA development board.



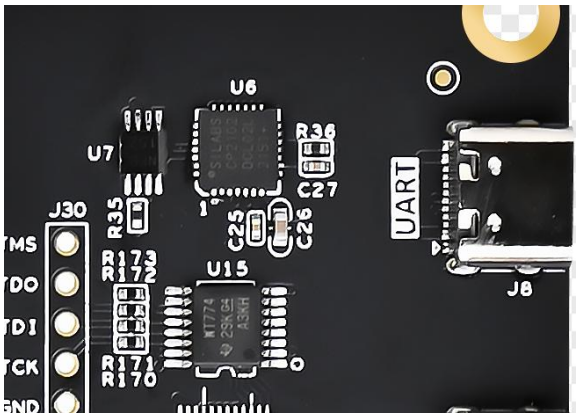
Part 4.4: USB to UART

The FPGA carrier board uses "**Silicon Labs CP2102GM**" chip to realize USB to UART, and the USB interface adopts "**TypeC**". Users only need to use a Micro USB cable to connect to the PC for serial communication.

The "**TX/RX**" signal of the UART is connected with the "**BANK84**" of the "**FPGA**", and the interface level is 3.3V, so the serial port interface adopts the level conversion to 3.3V and connects with the serial port chip.

The following is the signal correspondence table and schematic, the TX/RX direction is defined for the FPGA side.

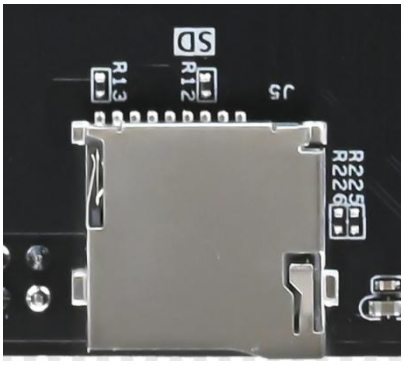
UART0 Pin	Pin Name	Pin Position
UART_TX	IO_5P_84	AC13
UART_RX	IO_5N_84	AC14



Part 4.5: SD Card

A SD card holder is placed on the FPGA carrier board (on the bottom of the board), which can be used for "**SD card**" startup, and is also convenient for users to debug or store files. The circuit interface level is "**3.3V**", the SD card signal is connected to the "BANK87" of the FPGA. The following is the signal correspondence, the detailed circuit can refer to the schematic diagram of the development board.

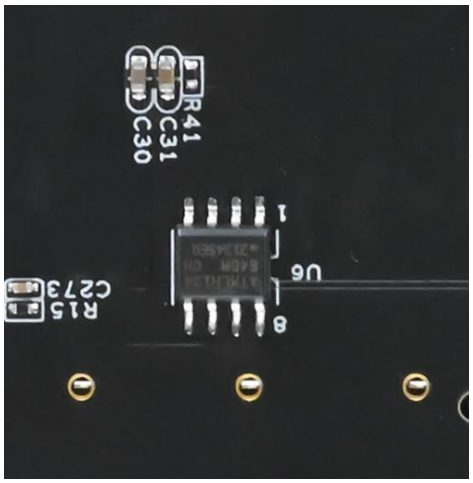
SD Card Pin	Pin Name	Pin Position
SD-CLK	IO_10P_87	C12
SD-CMD	IO_10N_87	B12
SD-DATA0	IO_5P_87	G12
SD-DATA1	IO_5N_87	F12
SD-DATA2	IO_6P_87	F14
SD-DATA3	IO_6N_87	F13



Part 4.6: E2PROM

The **64Kbit EEPROM** chip is placed on the FPGA carrier board, the model is AT24C64D-SSHM-T Connect with **BANK84** of **FPGA** through **IIC** bus, the interface level is 3.3V. The **EEPROM** read address is **0xA1**, and the write address is **0xA0**. The following is the pin assignment of the **EEPROM**, the detailed circuit can refer to the schematic diagram of the development board.

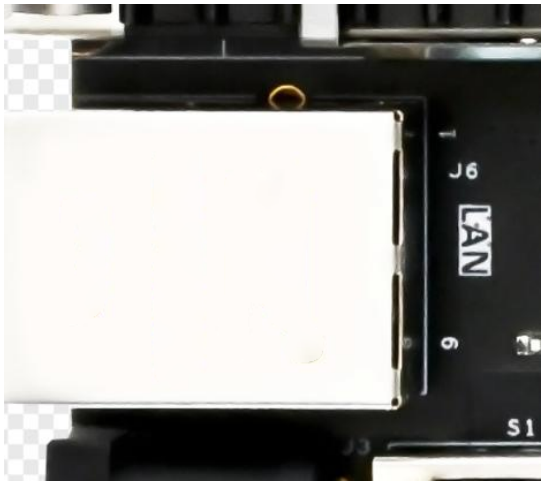
E2PROM	Pin Name	Pin Position
E2PROM_I2C_SCL	IO_6P_84	AB15
E2PROM_I2C_SDA	IO_6N_84	AB16



Part 4.7: Gigabit Ethernet

The FPGA carrier board are designed with one way Gigabit Ethernet. The Ethernet chip and **FPGA** are interconnected through the **RGMII** interface, and the Ethernet chip is interconnected with the FPGA through the RGMII interface to BANK65/87, the interface level is 1.8V. Connect the corresponding pins as shown in the table below, the address of the network port is **PHY_AD[2:0]=001**, you can refer to the schematic for the detailed circuit.

RMGII Signal	Pin Name	Pin Position
GTX_CLK	IO_24P_65	N21
TX_EN	IO_24N_65	N22
TXD0	IO_21P_65	R20
TXD1	IO_21N_65	R21
TXD2	IO_6P_65	W19
TXD3	IO_6N_65	W20
RX_CLK	IO_11P_GC_65	V23
RX_DV	IO_11N_GC_65	W23
RXD0	IO_18P_65	R25
RXD1	IO_18N_65	R26
RXD2	IO_15P_65	N24
RXD3	IO_15N_65	P24
MDC	IO_11P_87	A13
MDIO	IO_11N_87	A12



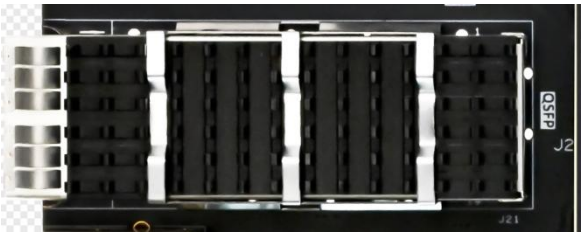
Part 4.8: QSFP28 Interface

Four 100G QSFP28 interfaces are designed on the FPGA carrier board. The interface signals are connected to the **BANK84/BANK226** of the **FPGA**. For details, please refer to the schematic.

The following is the pin assignment of **QSFP28**, the detailed circuit can refer to the schematic of the FPGA development board.

QSFP PIN	Pin Name	Pin Position
QSFP1-TX-P0	MGT_TX_P0_226	N5
QSFP1-TX-N0	MGT_TX_N0_226	N4
QSFP1-TX-P1	MGT_TX_P1_226	L5
QSFP1-TX-N1	MGT_TX_N1_226	L4
QSFP1-TX-P2	MGT_TX_P2_226	J5
QSFP1-TX-N2	MGT_TX_N2_226	J4
QSFP1-TX-P3	MGT_TX_P3_226	G5
QSFP1-TX-N3	MGT_TX_N3_226	G4

QSFP1-RX-P0	MGT_RX_P0_226	M2
QSFP1-RX-N0	MGT_RX_N0_226	M1
QSFP1-RX-P1	MGT_RX_P1_226	K2
QSFP1-RX-N1	MGT_RX_N1_226	K1
QSFP1-RX-P2	MGT_RX_P2_226	H2
QSFP1-RX-N2	MGT_RX_N2_226	H1
QSFP1-RX-P3	MGT_RX_P3_226	F2
QSFP1-RX-N3	MGT_RX_N3_226	F1
QSFP1_LPMODE	IO_10N_84	W15
QSFP1_I2C_SCL	IO_7P_84	Y15
QSFP1_I2C_SDA	IO_7N_84	AA15



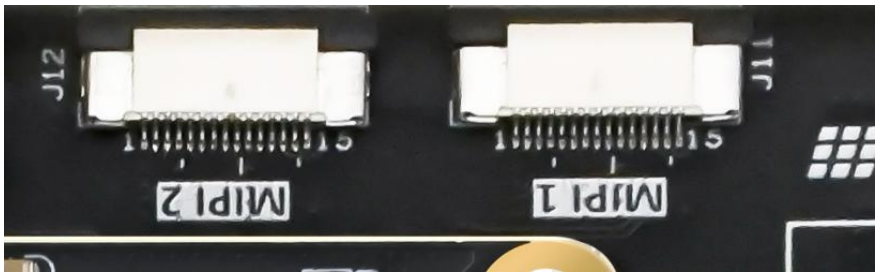
Part 4.9: MIPI Interface

Two MIPI interfaces are designed on the fpga carrier board, the pin definitions are listed in the table below, and you can refer to the schematic.

MIPI1 Signal	Pin Name	Pin Position
MIPI1_D_P0	IO_4P_65	V21
MIPI1_D_N0	IO_4N_65	V22
MIPI1_D_P1	IO_3P_65	T20
MIPI1_D_N1	IO_3N_65	U20
MIPI1_CLK_P	IO_1P_65	U19
MIPI1_CLK_N	IO_1N_65	V19
CAM1_RST	IO_12N_87	A14
CAM1_CLK	IO_12P_87	B14
CAM1_SCL	IO_1P_87	J12
CAM1_SDA	IO_1N_87	H12

MIPI2 Signal	Pin Name	Pin Position
MIPI2_D_P0	IO_20P_65	P20
MIPI2_D_N0	IO_20N_65	P21
MIPI2_D_P1	IO_23P_65	N19
MIPI2_D_N1	IO_23N_65	P19
MIPI2_CLK_P	IO_22P_65	N23

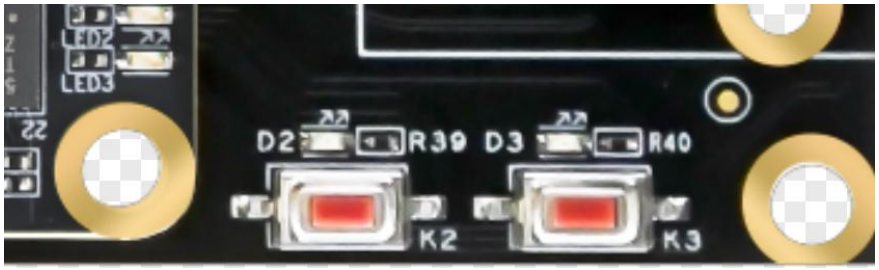
MIPI2_CLK_N	IO_22N_65	P23
CAM2_RST	IO_L7N_HDGC_87	E12
CAM2_CLK	IO_L7P_HDGC_87	E13
CAM2_SCL	IO_L8P_HDGC_87	D14
CAM2_SDA	IO_L8N_HDGC_87	D13



Part 4.10: LED

Two LEDs are designed on the fpga carrier board, the pin definitions are listed in the table below, and you can refer to the schematic.

LED Bits	Pin Name	Pin Position
LED1	IO-8P-84	AA14
LED2	IO-8N-84	AB14

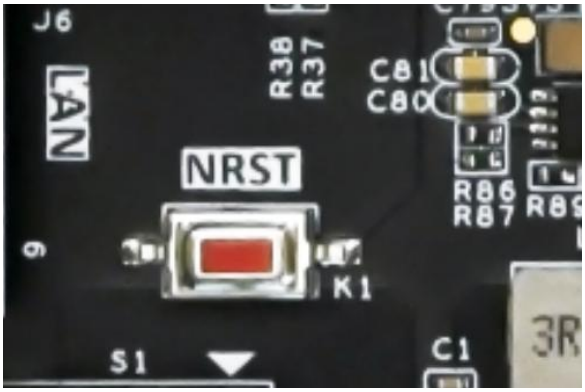


Part 4.11: KEY

The FPGA development board is designed with two user KEYs and one Reset Key. The KEY defaults to a high level, and the KEY is pressed to a low level. The KEY is connected to the PL side,. The pin positions of the KEYs are as follows.

LED Bits	Pin Name	Pin Position
KEY1	IO-2P-84	AE13
KEY2	IO-2N-84	AF13
SYS_nRST	IO-4N-84	AD14





Part 4.12: 40P 2.54mm Expansion Port

One 40P 2.54mm pitch simple horn socket is designed on the FPGA development board , which are used to expand the signal connection. The signals are connected to the FPGA's BANK86/87 at a level of 3.3V. The following table indicates the chip position where the signal is located. For the detailed connection relationship, please refer to the schematic diagram.

JM1 Signal Sequence	Pin Name	Pin Position	JM1 Signal Sequence	Pin Name	Pin Position
5	IO_L5P_HDGC_86	G10	6	IO_L7P_HDGC_86	E11
7	IO_L5N_HDGC _86	G9	8	IO_L7N_HDGC_86	E10
9	IO_L6P_HDGC _86	F10	10	IO_L8P_HDGC_86	D11
11	IO_L6N_HDGC _86	F9	12	IO_L8N_HDGC_86	D10
13	IO_L10P_86	B9	14	IO_L12P_86	C11
15	IO_L10N_86	A9	16	IO_L12N_86	B11
17	IO_L11P_86	B10	18	IO_L9P_86	D9
19	IO_L11N_86	A10	20	IO_L9N_86	C9
21	IO_L4P_86	H11	22	IO_L2P_86	J11
23	IO_L4N_86	G11	24	IO_L2N_86	J10
25	IO_3P_86	J9	26	IO_1P_86	K10
27	IO_L3N_86	H9	28	IO_L1N_86	K9
29	IO_L4P_87	J15	30	IO_L2P_87	J13
31	IO_L4N_87	J14	32	IO_L2N_87	H13
37	IO_L9P_87	C14	38	IO_L3P_87	H14
39	IO_L9N_87	C13	40	IO_L3N_87	G14

Part 4.13: FMC Expansion Port

One **FMC HPC** connector is designed on the FPGA carrier board, However, due to the limited number of pins on the chip, not all of them are actually connected, only 4 pairs of MGT and LA signals are connected, and the following table lists the signal correspondences.Refer to the schematicfor details

Number	FMC HPC Pin	Pin Name	Pin Position
A2	DP1_M2C_P	MGT_RX_P1_227	C4
A3	DP1_M2C_N	MGT_RX_N1_227	C3
A6	DP2_M2C_P	MGT_RX_P2_227	B2
A7	DP2_M2C_N	MGT_RX_N2_227	B1
A10	DP3_M2C_P	MGT_RX_P3_227	A4
A11	DP3_M2C_N	MGT_RX_N3_227	A3
A22	DP1_C2M_P	MGT_TX_P1_227	E5
A23	DP1_C2M_N	MGT_TX_N1_227	E4
A26	DP2_C2M_P	MGT_TX_P2_227	D7
A27	DP2_C2M_N	MGT_TX_N2_227	D6
A30	DP3_C2M_P	MGT_TX_P3_227	B7
A31	DP3_C2M_N	MGT_TX_N3_227	B6
B20	GBTCLK1_M2C_P	MGT_CLK0_P_227	K7
B21	GBTCLK1_M2C_N	MGT_CLK0_N_227	K6
C2	DP0_C2M_P	MGT_TX_P0_227	F7
C3	DP0_C2M_N	MGT_TX_N0_227	F6
C6	DP0_M2C_P	MGT_RX_P0_227	D2
C7	DP0_M2C_N	MGT_RX_N0_227	D1
C10	LA06_P	IO_L3P_64	AF24
C11	LA06_N	IO_L3N_64	AF25
C14	LA10_P	IO_L6P_64	AB24
C15	LA10_N	IO_L6N_64	AC24
C18	LA14_P	IO_L23P_64	Y17
C19	LA14_N	IO_L23N_64	AA17
C22	LA18_P_CC	IO_L13P_MRCC_64	AD20
C23	LA18_N_CC	IO_L13N_MRCC_64	AE20
C26	LA27_P	IO_L16P_65	U26
C27	LA27_N	IO_L16N_65	V26
C30	SCL	IO_L11P_84	Y13
C31	SDA	IO_L11N_84	AA13
D4	GBTCLK0_M2C_P	MGT_CLK0_P_226	P7
D5	GBTCLK0_M2C_N	MGT_CLK0_N_226	P6
D8	LA01_P_CC	IO_L11P_SRCC_64	AD21
D9	LA01_N_CC	IO_L11N_SRCC_64	AE21
D11	LA05_P	IO_L1P_64	AE25
D12	LA05_N	IO_L1N_64	AE26
D14	LA09_P	IO_L2P_64	AB25
D15	LA09_N	IO_L2N_64	AB26

D17	LA13_P	IO_L24P_64	Y18
D18	LA13_N	IO_L24N_64	AA18
D20	LA17_P_CC	IO_L12P_MRCC_64	AB21
D21	LA17_N_CC	IO_L12N_MRCC_64	AC21
D23	LA23_P	IO_L9P_64	AC22
D24	LA23_N	IO_L9N_64	AC23
D26	LA26_P	IO_L10P_65	W25
D27	LA26_N	IO_L10N_65	W26
G2	CLK1_M2C_P	IO_L14P_SRCC_65	T25
G3	CLK1_M2C_N	IO_L14N_SRCC_65	U25
G6	LA00_P_CC	IO_L14P_SRCC_64	AC19
G7	LA00_N_CC	IO_L14N_SRCC_64	AD19
G9	LA03_P	IO_L18P_64	AD16
G10	LA03_N	IO_L18N_64	AE16
G12	LA08_P	IO_L7P_64	AE22
G13	LA08_N	IO_L7N_64	AF22
G15	LA12_P	IO_L8P_64	AD23
G16	LA12_N	IO_L8N_64	AE23
G18	LA16_P	IO_L5P_64	AD24
G19	LA16_N	IO_L5N_64	AD25
G21	LA20_P	IO_L4P_64	AC26
G22	LA20_N	IO_L4N_64	AD26
G24	LA22_P	IO_L19P_64	Y20
G25	LA22_N	IO_L19N_64	Y21
G27	LA25_P	IO_L5P_65	T22
G28	LA25_N	IO_L5N_65	T23
G30	LA29_P	IO_L1P_65	U19
G31	LA29_N	IO_L1N_65	V19
G33	LA31_P	IO_L4P_65	V21
G34	LA31_N	IO_L4N_65	V22
G36	LA33_P	IO_L8P_65	Y25
G37	LA33_N	IO_L8N_65	Y26
H4	CLK0_M2C_P	IO_L12P_MRCC_65	V24
H5	CLK0_M2C_N	IO_L12N_MRCC_65	W24
H7	LA02_P	IO_L17P_64	AE17
H8	LA02_N	IO_L17N_64	AF17
H10	LA04_P	IO_L15P_64	AF18
H11	LA04_N	IO_L15N_64	AF19
H13	LA07_P	IO_L16P_64	AC18
H14	LA07_N	IO_L16N_64	AD18
H16	LA11_P	IO_L22P_64	AB17
H17	LA11_N	IO_L22N_64	AC17
H19	LA15_P	IO_L20P_64	AA19
H20	LA15_N	IO_L20N_64	AB19
H22	LA19_P	IO_L21P_64	AA20
H23	LA19_N	IO_L21N_64	AB20
H25	LA21_P	IO_L10P_64	AA22
H26	LA21_N	IO_L10N_64	AB22

H28	LA24_P	IO_L7P_65	Y22
H29	LA24_N	IO_L7N_65	Y23
H31	LA28_P	IO_L9P_65	AA24
H32	LA28_N	IO_L9N_65	AA25
H34	LA30_P	IO_L2P_65	U21
H35	LA30_N	IO_L2N_65	U22
H37	LA32_P	IO_L3P_65	T20
H38	LA32_N	IO_L3N_65	U20

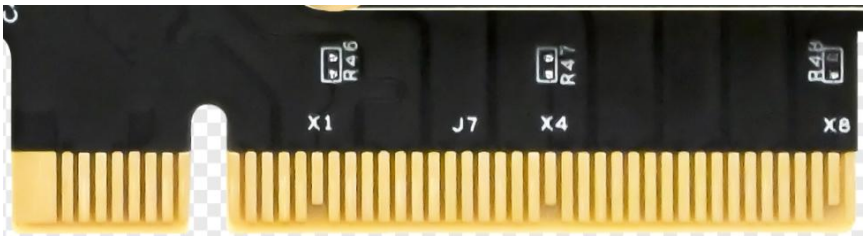


Part 4.14: PCIE 3.0 Interface

PCIE 3.0 Interface is designed on the FPGA carrier board, is x 8 interface, The following table lists the PCIE interface correspondences.

PCIE3.0	Pin Name	Pin Position
PERST_N	IO_4P_84	AD13
REF_CLK_P	MGT_CLK_P0_224	AB7
REF_CLK_N	MGT_CLK_N0_224	AB6
PER0_P	MGT_TX_P0_224	AF7
PER0_N	MGT_TX_N0_224	AF6
PER1_P	MGT_TX_P1_224	AE9
PER1_N	MGT_TX_N1_224	AE8
PER2_P	MGT_TX_P2_224	AD7
PER2_N	MGT_TX_N2_224	AD6
PER3_P	MGT_TX_P3_224	AC5
PER3_N	MGT_TX_N3_224	AC4
PER4_P	MGT_TX_P0_225	AA5
PER4_N	MGT_TX_N0_225	AA4
PER5_P	MGT_TX_P1_225	W5
PER5_N	MGT_TX_N1_225	W4
PER6_P	MGT_TX_P2_225	U5
PER6_N	MGT_TX_N2_225	U4
PER7_P	MGT_TX_P3_225	R5
PER7_N	MGT_TX_N3_225	R4
PET0_P	MGT_RX_P0_224	AF2
PET0_N	MGT_RX_N0_224	AF1
PET1_P	MGT_RX_P1_224	AE4
PET1_N	MGT_RX_N1_224	AE3
PET2_P	MGT_RX_P2_224	AD2
PET2_N	MGT_RX_N2_224	AD1

PET3_P	MGT_RX_P3_224	AB2
PET3_N	MGT_RX_N3_224	AB1
PET4_P	MGT_RX_P0_225	Y2
PET4_N	MGT_RX_N0_225	Y1
PET5_P	MGT_RX_P1_225	V2
PET5_N	MGT_RX_N1_225	V1
PET6_P	MGT_RX_P2_225	T2
PET6_N	MGT_RX_N2_225	T1
PET7_P	MGT_RX_P3_225	P2
PET7_N	MGT_RX_N3_225	P1



Part 4.15: USB to JTAG Programmer

USB to **JTAG** Programmer onboard is designed on the FPGA carrier board. After installing the **Vivado** software, use a **USB** cable to connect the USB port corresponding to JTAG. You can realize debugging and downloading, which is very convenient. The following is the location of the interface on the FPGA development board.

