Kintex UltraScale FPGA Board

CRKU040 | CRKU060 | CRKU095

User Manual

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Version Records:

Data	Version	Description
2020.5.08	V1.0	initial version

This tutorial will continue to revise, optimize and increase based on the actual Experience, that is to provide you with more and better Demos.

If you find some errors or any suggestion, contact with us.

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Par1: Kintex UltraScale series Introduction

Kintex™ UltraScale™ devices provide the best price/performance/watt at 20nm and include the highest signal processing bandwidth in a mid-range device, next- generation transceivers, and low-cost packaging for an optimum blend of capability and cost-effectiveness. The family is ideal for packet processing in 100G networking and data center applications as well as DSP-intensive processing needed in next- generation medical imaging, 8k4k video, and heterogeneous wireless infrastructure.

Value	Deliverables
Programmable System Integration	• Up to 1.5M System Logic Cells leveraging 2nd generation 3D IC • Multiple integrated PCI Express® Gen3 cores
Increased System Performance	• 8.2 TeraMACs of DSP compute performance • Up to two speed-grade improvement with high utilization • 16G backplane-capable transceivers, up to 64 per device • 2,400Mb/s DDR4 for robust operation over varying PVT
BOM Cost Reduction	• System integration reduces application BOM cost by up to 60% • 12.5Gb/s transceivers in slowest speed grade • 2,400Mb/s DDR4 in a mid-speed grade • VCXO integration reduces clocking component cost
Total Power Reduction	• Up to 40% lower power vs. previous generation • Fine granular clock gating with UltraScale devices ASIC-like clocking • Enhanced system logic cell packing reduces dynamic power
Accelerated Design Productivity	• Footprint compatibility with Virtex™ UltraScale devices for scalability • Co-optimized with Vivado™ Design Suite for rapid design closure

Kintex® UltraScale™ device resources are listed below:

Kintex UltraScale Product Table

XCKU025 XCKU035 XCKU040 **XCKU060** XCKU085 XCKU095 XCKU115

COMPARE / Reset	XCKU035	XCKU040	XCKU060	XCKU085
System Logic Cells (K)	444	530	726	1,088
DSP Slices	1,700	1,920	2,760	4,100
Block RAM (Mb)	19.0	21.1	38.0	56.9
16.3Gb/s Transceivers	16	20	32	56
I/O Pins	520	520	624	676

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Part 2: CR-KU060/060/095 FPGA Board

Overview

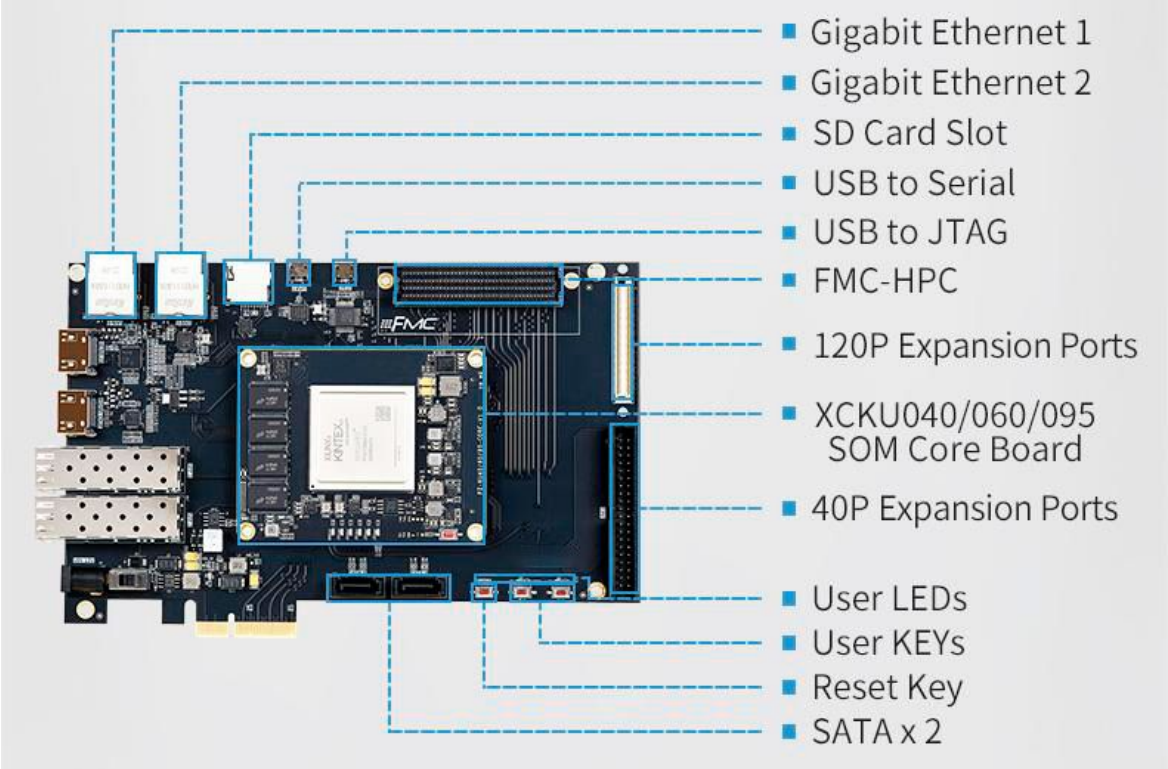
Part 2.1: Board Introduction

The Kintex UltraScale series FPGA development board has three versions, namely CRKU040, CRKU060, CRKU095. The peripherals of the three versions are fully compatible, and the only difference is the logic capacity of the main chip FPGA.

The Kintex UltraScale series FPGA development board adopts the mode of "core board + Carrier board". The core board plugs into the carrier board connector through four 120P high-speed connectors. More flexible in use. You can use the core board for both learning and project development.

The FPGA development board integrates rich peripheral resources and provides detailed demos. The board also incorporates the JTAG debugger, a MicroUSB cable, and a 12V power supply to get the board working. More convenient for users.

The form factors of the development board is 195mm x 115mm. A fixed hole is placed at each of the four corners of the core board for mounting support columns or fixing veneers. The aperture is 3.5mm.



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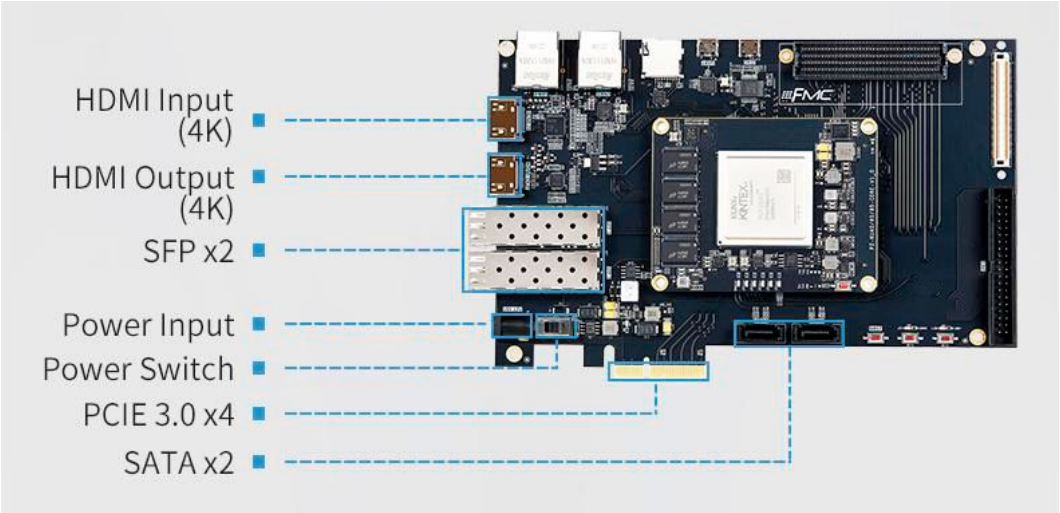

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Part 2.2: FPGA Board Resources and Block Diagram

The onboard resources of the FPGA development board are listed in the table and block diagram below, and the functions we have included can be seen from the table below.

FPGA Chip	XCKU040-2FFVA1156I	XCKU060-2FFVA1156I	XCKU095-2FFVA1156I
Logic Cells（K）	530250	725550	1176000
LUT	242400	331680	537600
Flip-Flops	484800	663630	1075200
BLOCK ROM	21.1Mb	38Mb	59.1Mb
DSP Slices	1920	2760	768
QSPI FLASH	32MB, stores boot files and user files		
E2PROM	64Kb		
Start-up Method	Default QSPI startup		
Serial Port	1		
SD Card Slot	1		
Programmer (On-board)	1		
HDMI Input (4K)	1		
HDMI Output (4K)	1		
Gigabit Ethernet	2		
User LED/ User Key	2 / 2		
SFP Interface	2		
PCIE3.0	x 4 Interface		
40P Expansion Port	32 Single-ended/16 Pairs of Differential (3.3V)		
120P Expansion Port	48 single-ended/24 differential Pairs (1.2/1.8V Adjustable)		
FMC-HPC Port	Signal Definition Contact Customer Service		
Voltage/Current	12V / 3A		
Technology	83.8x64.8mm, Immersion Gold Process		

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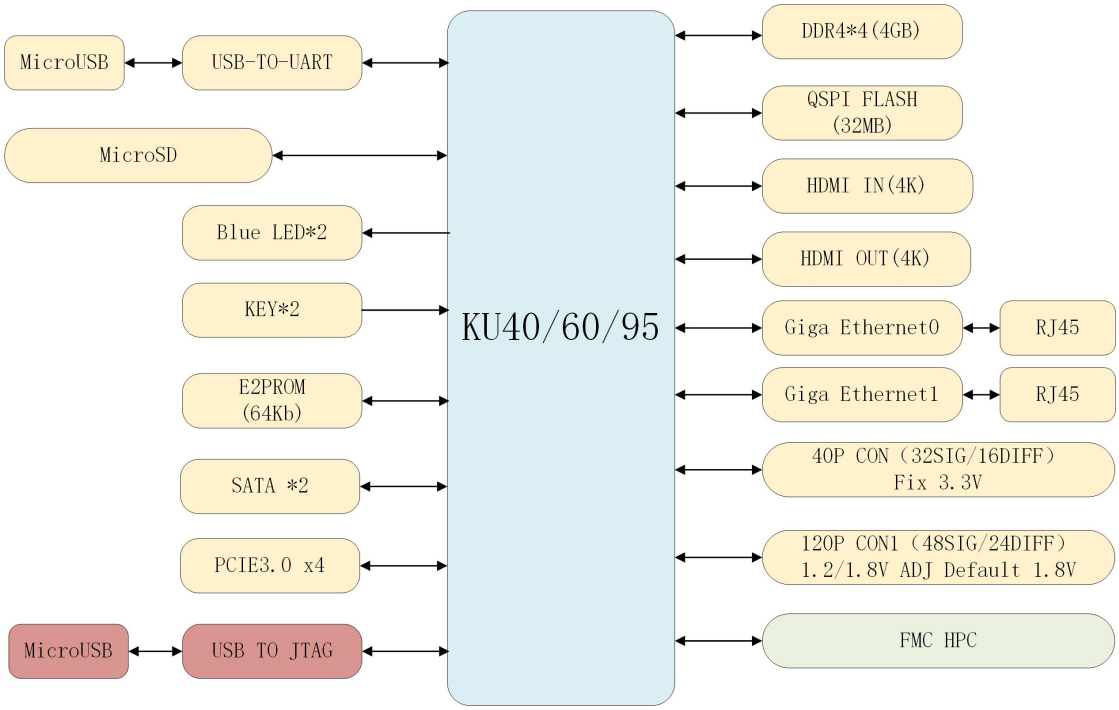

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Part 3: CR-KU040/060/095 SOM Core Board

Overview

Part 3.1: SOM Introduction

The CR-KU40/60/95 SOM core board adopts the XCKU040-2FFVA1156I/XCKU060-2FFVA1156I/XCKU095-2FFVA1156I chip of XILINX Kintex UltraScale+ family chips as the main controller. The core board is connected to the carrier board with three 0.5mm pitch 168P gold-plated high-speed connectors, and four 3.5mm fixing holes are placed on the four feet of the core board. This hole can be fastened with the carrier board by screws, which ensures stable operation in the environment of strong vibration.

KU family core boards have been tested for a long time in high and low temperatures, and the indicators have reached industrial standards, meeting the working environment of -40-85℃.

In addition, the carrier board that supports the KU series core board, provide a wealth of peripheral interfaces and detailed demos source code, greatly reducing the user's learning time and speed up the product development.

Part 3.2: SOM Specification

Kintex Ultrascale 040/060/095 Industrial Grade SOM Specification			
FPGA Chip	XCKU040-2FFVA1156I	XCKU060-2FFVA1156I	XCKU095-2FFVA1156I
Logic Cells（K）	530250	725550	1176000
LUT	242400	331680	537600
Flip-Flops	484800	663630	1075200
BLOCK ROM	21.1Mb	38Mb	59.1Mb
DSP Slices	1920	2760	768
DDR4	4GB Capacity/64bit bit width		
QSPI FLASH	Total 2 way, 64MB (32MB * 2)		
Start-up Mode	JTAG/QSPI, default QSPI boot		
Gigabit Ethernet	1		
User LEDs	5		
Reset Key	1		
GTH Interface	20 Pairs of TX/RX		
Number of IOs	Total 296 IOs HR: 8 single-ended (Fixed 3.3V Level)		

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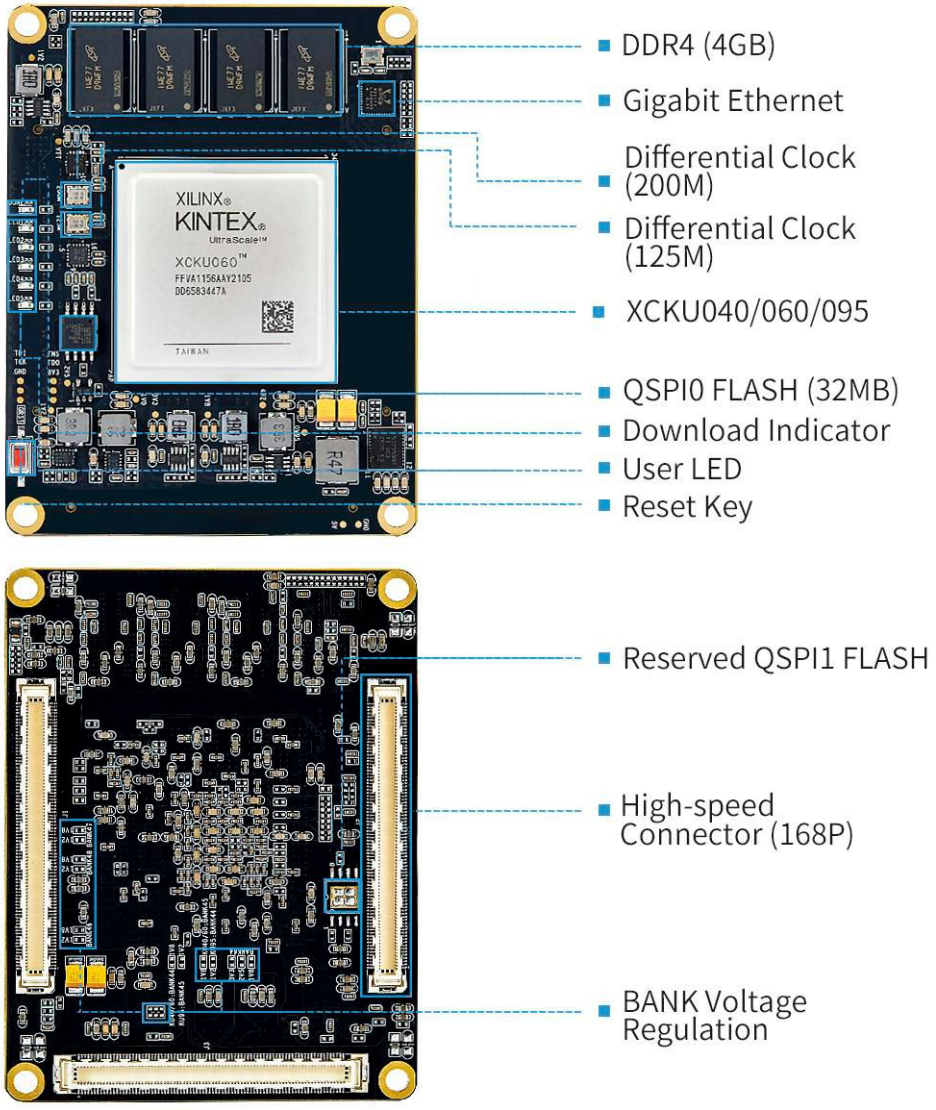
	HP: 24 differential pairs / 48 single-ended (1.8/2.5/3.3 V Adjustable) HP: 120 differential pairs / 240 single-ended (1.2/1.8V Adjustable)
Voltage/Current	5V/6A
Form Factors, Technology	83.8x64.8mm, Immersion Gold Process, 168P Connectors X 3
Connector Height	4mm

Part 3.3: Product Appearance

As shown in the figure below, the position of each main electronic component on the core board is marked, which is convenient for users to view and identify.



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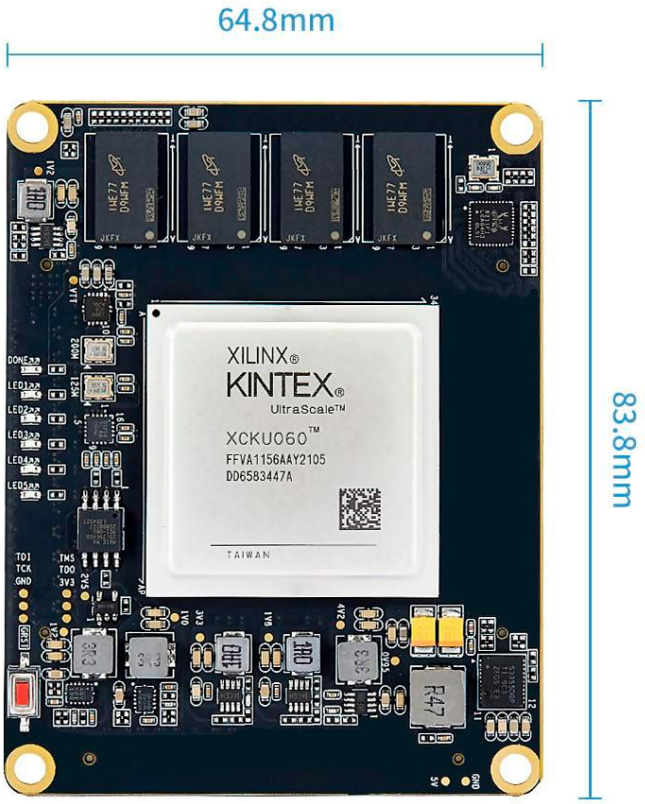
Part 3.4: SOM Form Factors

The Form Factors of the core board is 83.8mm x 64.8mm.For the height we have made a detailed description to facilitate the user in customizing the shell for reference. The height of the connector between the core board and the carrier board is 4mm, the thickness of the core board PCB is 1.75mm, and the maximum height of the front device of the core board is 3.5mm. For users who use our customized heat sink system (heatsink + fan), also need to consider the height of the heat sink system, the thickness of the system is 7mm, and the height of the support column between the system and the core board is 5mm. The following picture is the form factors of the core board.





Part 3.5: Power Connection

The power supply voltage of the core board is 5V, and the power input pins are reserved in the opposite corners of the core board. The power supply pins have been made connected inside the

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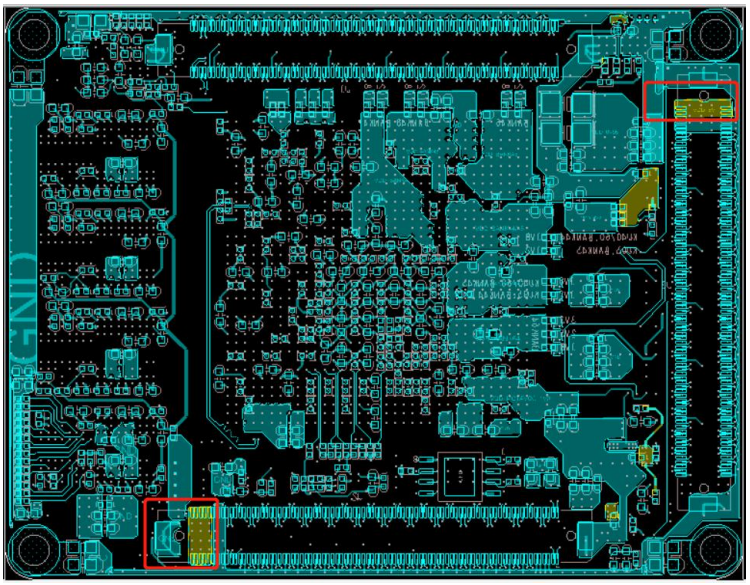
module, which is designed to facilitate the power access of the carrier board. When designing the carrier board, only one corner of the power supply needs to be connected and the core board can work.

The power connection needs to be connected with copper and enough through holes are made to ensure the power flow capacity. All GND signals on the core board need to be connected to the carrier board, and each GND is connected to the carrier board through two vias. The limit current of the core board power supply is 5V/6A, so the external power supply needs to consider the limit current to ensure the stable operation of the core board.

The output voltage of the power supply to the module needs to be stable. Add a first-level DCDC power conversion to the module power input, from high voltage to 5V, and the DCDC current output capacity can be about 6A. For example, you can refer to the power chip TPS56628DDAR. Two **220uF/25V** capacitors should be placed at the power input of the module to ensure power quality.



Part 3.6: Clock

The core board is placed on two active differential crystal, 200M clock for the logic side to provide a differential clock, 125M for the GTX interface to provide a differential clock. The following figure, 200M differential clock into the 12P/12N pin of the KU40/60 BANK67 or KU95 BANK68 , the corresponding pin location is D24/C24. 125M clock did BUF converted into three ways respectively to Y6/Y5, T6/T5, M6/M5 position of BANK225/226/227.

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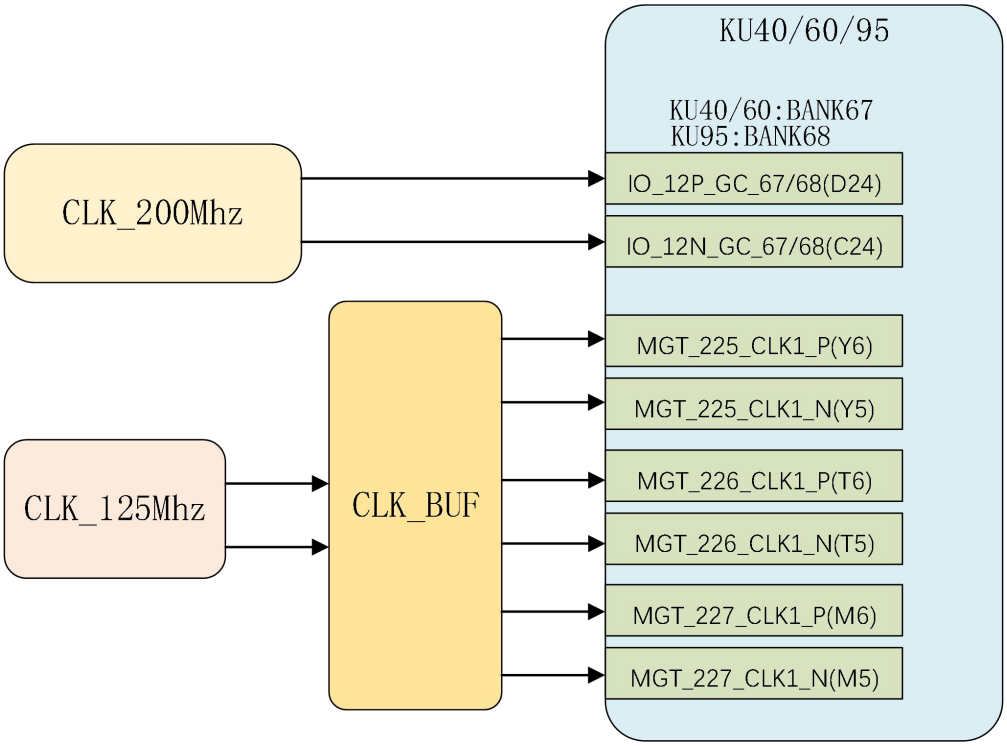
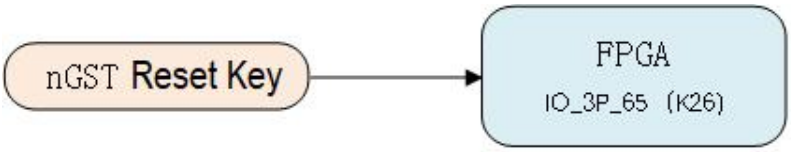


Part 3.7: Global Reset

The Core board reserved a reset key for debugging use, this reset key using RC circuit, reset is not sufficient, only as a debugging use, the key is connected to the FPGA BANK65, the corresponding pin is IO_13P_65 (K26).

The actual product needs to add a reset circuit, you can use a special reset chip on the carrier board, such as MAX811, or other longer reset time chip.





Part 3.8: Boot Mode Selection

The boot mode has been set on the core board, and the system defaults to the "**Master SPI**" boot

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mode.

The core board supports two startup modes, respectively, JTAG, QSPI Flash. the default is QSPI Flash startup, JTAG connection automatically recognised without the use of dip switches to switch between JTAG, QSPI mode.

BOOT MODE	M2	M1	M0
JTAG	1	0	1
M SPI	0	0	1

Part 3.9: Network Port Connection

The Gigabit Ethernet chip RTL8211FI-CG is placed on the core board. The Ethernet chip and the FPGA chip are interconnected through the RGMII interface. The corresponding pins are shown in the table below. Ethernet external connection only needs an RJ45 with a transformer to use, the chip address PHY_AD[2:0]=001, reset pin is low active. The connection schematic diagram can refer to the following figure (the product circuit needs to add an ESD protection circuit).

RMGII Signal	Pin Name	Pin Position
TX_CLK	IO_14P_MRCC_65	P24
TXD0	IO_15P_65	T27
TXD1	IO_15N_65	R27
TXD2	IO_16P_65	T24
TXD3	IO_16N_65	T25
TX_EN	IO_17P_65	R25
RX_CLK	IO_13P_MRCC_65	P26
RXD0	IO_17N_65	R26
RXD1	IO_18P_65	R23
RXD2	IO_18N_65	P23
RXD3	IO_19P_65	N22
RX_CTL	IO_19N_65	M22
PHY_nRST	IO_13N_SRCC_65	N26
MDC	IO_20P_65	P20
MDIO	IO_20N_65	P21

Part 3.10: QSPI FLASH

The FPGA development board is designed with two-way QSPI FLASH, the default chip QSPI0, QSPI1 does not installed. X4 operation mode, the capacity of 32MB, model MX25L25645GM2I-08G, used to store the boot file or user files. The following table shows the pin positions of the two QSPIs.

QSPI0 FLASH Pin	FPGA Pin Name	Pin Position

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DATA0	D00_MOSI	AC7
DATA1	D01_DIN	AB7
DATA2	D02	AA7
DATA3	D03	Y7
QSPI_CS	RDWR_FCS_B	U7
QSPI_CLK	CCLK	AA9
QSPI1 FLASH Pin	**FPGA Pin Name**	**Pin Position**
DATA0	IO_L22P_65	M20
DATA1	IO_L22N_65	L20
DATA2	IO_L21P_65	R21
DATA3	IO_L21N_65	R22
QSPI_CS	IO_L2N_65	G26

Part 3.11: On-board LED

In order to facilitate debugging, five LEDs are placed on the core board. The pin positions of the LEDs are as shown in the table below. When the pin outputs a high level, the LED lights up, and the low level LED goes out.

Number	Pin Name	Pin Position
LED1	IO_T0U_65	H23
LED2	IO_T2U_65	N27
LED3	IO_L23P_65	N21
LED4	IO_L23N_65	M21
LED5	IO_L2P_65	G25

Part 3.12: BANK Interface Level Selection

The external BANK on the core board are BANK44/45/46/47/48/64, the IO of these BANK can be independently adjusted voltage. The BANK44/45/46/47/48 support 1.2V/1.8V level adjustment, the default level is 1.8V. BANK64 support 1.8V/2.5V/3.3V level adjustment, the default level is 3.3V, if you need to change the level, you only need to change the corresponding position resistor to achieve adjustment, such as the 3.3V level to 1.8V. Just change the resistor of 3.3V position to 1.8V position. The core board is marked with the BANK level adjustment resistor position, as shown below.

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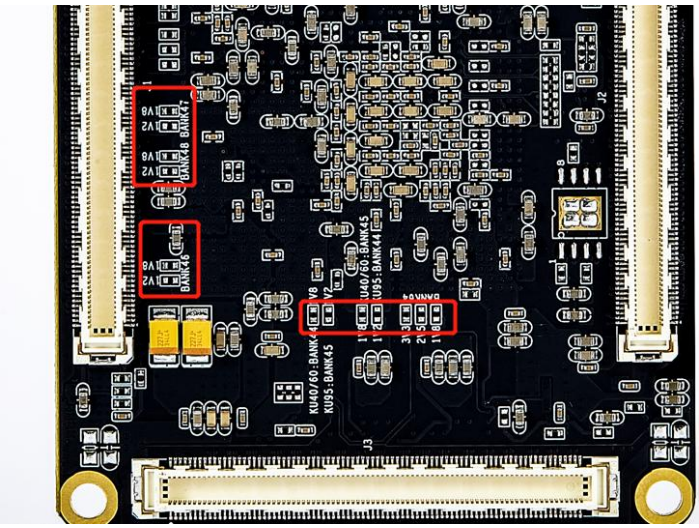

Part 3.13: DDR4 Pin Connection

The core board contains four industrial-grade DDR4 chips with a single capacity of 1GB and a total capacity of 4GB. The model is "**MT40A512M16LY-062E IT:E**", DDR4 pin allocation see the following table.

DDR4 Pin	FPGA Pin Name	Pin Position
DDR4_D0	IO-L6N-66	D10
DDR4_D1	IO-L3N-66	C8
DDR4_D2	IO-L5P-66	D9
DDR4_D3	IO-L5N-66	C9
DDR4_D4	IO-L6P-66	E10
DDR4_D5	IO-L3P-66	D8
DDR4_D6	IO-L2N-66	A9
DDR4_D7	IO-L2P-66	B9
DDR4_DM0	IO-L1P-66	F8
DDR4_DQS_P0	IO-L4P-66	B10
DDR4_DQS_N0	IO-L4N-66	A10
DDR4_D8	IO-L12P-66	G10
DDR4_D9	IO-L9P-66	J8
DDR4_D10	IO-L11N-66	F9
DDR4_D11	IO-L9N-66	H8
DDR4_D12	IO-L12N-66	F10
DDR4_D13	IO-L8P-66	J9
DDR4_D14	IO-L11P-66	G9
DDR4_D15	IO-L8N-66	H9
DDR4_DM1	IO-L7P-66	L8

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DDR4_DQS_P1	IO-L10P-66	K10
DDR4_DQS_N1	IO-L10N-66	J10
DDR4_D16	IO-L14P-66	H12
DDR4_D17	IO-L17N-66	K12
DDR4_D18	IO-L14N-66	G12
DDR4_D19	IO-L15P-66	K11
DDR4_D20	IO-L18N-66	H13
DDR4_D21	IO-L17P-66	L12
DDR4_D22	IO-L18P-66	J13
DDR4_D23	IO-L15N-66	J11
DDR4_DM2	IO-L13P-66	H11
DDR4_DQS_P2	IO-L16P-66	L13
DDR4_DQS_N2	IO-L16N-66	K13
DDR4_D24	IO-L23P-66	A13
DDR4_D25	IO-L21P-66	C11
DDR4_D26	IO-L24N-66	C13
DDR4_D27	IO-L21N-66	B11
DDR4_D28	IO-L24P-66	D13
DDR4_D29	IO-L20P-66	C12
DDR4_D30	IO-L20N-66	B12
DDR4_D31	IO-L23N-66	A12
DDR4_DM3	IO-L19P-66	E11
DDR4_DQS_P3	IO-L22P-66	F13
DDR4_DQS_N3	IO-L22N-66	E13
DDR4_D32	IO-L2P-68	A19
DDR4_D33	IO-L5N-68	B16
DDR4_D34	IO-L6P-68	C18
DDR4_D35	IO-L5P-68	B17
DDR4_D36	IO-L2N-68	A18
DDR4_D37	IO-L3P-68	B15
DDR4_D38	IO-L6N-68	C17
DDR4_D39	IO-L3N-68	A15
DDR4_DM4	IO-L1P-68	B14
DDR4_DQS_P4	IO-L4P-68	C19
DDR4_DQS_N4	IO-L4N-68	B19
DDR4_D40	IO-L12P-68	E18
DDR4_D41	IO-L8P-68	E15
DDR4_D42	IO-L11P-68	E16
DDR4_D43	IO-L9P-68	F15
DDR4_D44	IO-L12N-68	E17
DDR4_D45	IO-L8N-68	D15
DDR4_D46	IO-L11N-68	D16

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DDR4_D47	IO-L9N-68	F14
DDR4_DM5	IO-L7P-68	D14
DDR4_DQS_P5	IO-L10P-68	D19
DDR4_DQS_N5	IO-L10N-68	D18
DDR4_D48	IO-L18N-68	H18
DDR4_D49	IO-L17N-68	H16
DDR4_D50	IO-L17P-68	H17
DDR4_D51	IO-L15P-68	G15
DDR4_D52	IO-L18P-68	H19
DDR4_D53	IO-L14N-68	F17
DDR4_D54	IO-L14P-68	F18
DDR4_D55	IO-L15N-68	G14
DDR4_DM6	IO-L13P-68	G17
DDR4_DQS_P6	IO-L16P-68	G19
DDR4_DQS_N6	IO-L16N-68	F19
DDR4_D56	IO-L24P-68	L19
DDR4_D57	IO-L21N-68	K15
DDR4_D58	IO-L24N-68	L18
DDR4_D59	IO-L20N-68	K17
DDR4_D60	IO-L20P-68	K18
DDR4_D61	IO-L23N-68	J16
DDR4_D62	IO-L23P-68	K16
DDR4_D63	IO-L21P-68	L15
DDR4_DM7	IO-L19P-68	J15
DDR4_DQS_P7	IO-L22P-68	J19
DDR4_DQS_N7	IO-L22N-68	J18
DDR4_A0	IO-L16N-67	C22
DDR4_A1	IO-L19P-67	G24
DDR4_A2	IO-L3N-67	D29
DDR4_A3	IO-L6N-67	A28
DDR4_A4	IO-L14P-67	E22
DDR4_A5	IO-L4N-67	A29
DDR4_A6	IO-L17N-67	A20
DDR4_A7	IO-L6P-67	A27
DDR4_A8	IO-L21P-67	F23
DDR4_A9	IO-L5P-67	D28
DDR4_A10	IO-L17P-67	B20
DDR4_A11	IO-L18N-67	D21
DDR4_A12	IO-L7P-67	E26
DDR4_A13	IO-L3P-67	E28
DDR4_A14	IO-L20N-67	E21
DDR4_A15	IO-L21N-67	F24

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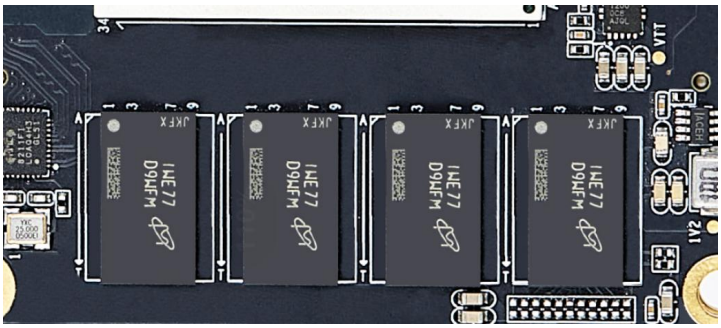
DDR4_A16	IO-L22P-67	G20
DDR4_BA0	IO-L20P-67	E20
DDR4_BA1	IO-L19N-67	F25
DDR4_BG0	IO-L15P-67	B21
DDR4_nCS	IO-L14N-67	E23
DDR4_ODT	IO-L18P-67	D20
DDR4_RESET	IO-L4P-67	B29
DDR4_CLK_P	IO-L13P-67	D23
DDR4_CLK_N	IO-L13N-67	C23
DDR4_CKE	IO-L16P-67	C21
DDR4_TEN	IO-L9N-67	B26
DDR4_nACT	IO-L8N-67	A25
DDR4_nALERT	IO-L9P-67	C26
DDR4_PARITY	IO-L8P-67	B25



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Part 4: CR-KU040/060/095 SOM Carrier Board

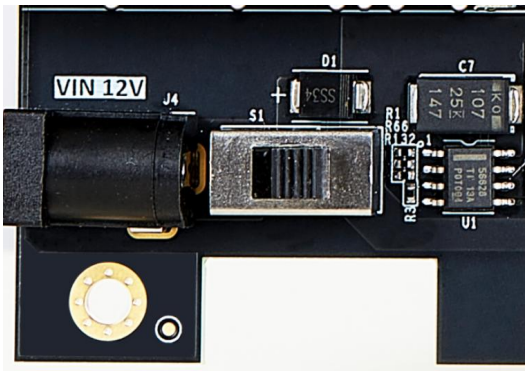
Overview

Part 4.1: Power Supply and BANK Voltage Regulation

The FPGA development board provides two power supply modes: PCIE interface and 12V/3A power adapter. The two power supply options can be selected by DIP switch S1 on the FPGA development board. If switch S1 is moved to a position close to the DC005 plug, the external adapter is used for power supply. If switch S1 is moved to the other side, the PCIE interface is powered.

After the 12V power supply enters the FPGA development board, it is converted into 5V/3.3V power supply through the secondary power supply, which is used by the core board and the internal and external peripherals of the board. Detailed circuit can refer to the schematic diagram of the FPGA development board.

In addition, the level of each BANK on the core board can be adjusted independently. If you need to adjust the voltage, you can adjust the resistance corresponding to the BANK. For details, refer to the Core Board user manual.



Part 4.2: Reset Circuit

A reset circuit is reserved on the FPGA Carrier board and the SOM core board respectively, the user can choose which one to use according to the actual use.

The core board reserved a reset key for debugging use, this reset key using the RC circuit, the reset is not sufficient, only as a debugging use, the key is connected to the BANK65 of the FPGA, the corresponding pin is IO_13P_65 (K26)

The reset pin on the development board is connected to the BANK64 of the FPGA, and the corresponding pin is IO_23P_17 (AJ9).

The actual product needs to add a reset circuit, you can use a special reset chip on the carrier board, such as MAX811, the user can make a choice according to need.

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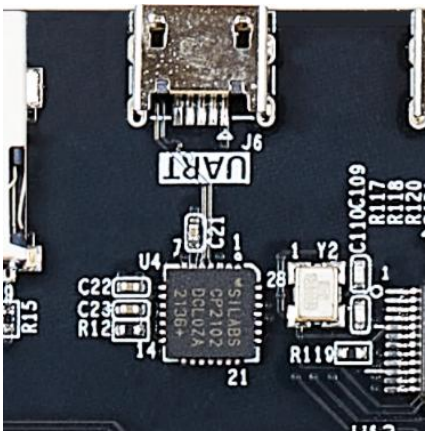
Part 4.3: USB to UART

The FPGA development board uses "**Silicon Labs CP2102GM**" chip to realize USB to UART, and the USB interface adopts "**Micro USB**". Users only need to use a Micro USB cable to connect to the PC for serial communication.

The "**TX/RX**" signal of the UART is connected with the "**BANK65**" of the "**FPGA**", and the interface level is 3.3V. The following is the signal correspondence table and schematic diagram, the TX/RX direction is defined on the FPGA side.

UART0 Pin	FPGA Pin Name	Pin Position
UART_TX	IO- PERSTN1-65	N23
UART_RX	IO-24P-65	K20



Part 4.4: SD Card

A TF card holder is placed on the FPGA development board, which is convenient for users to store files. The circuit interface level is "**3.3V**", the SD card signal is connected to the "BANK47" of the FPGA. The following is the signal correspondence table and schematic. The TX/RX direction is defined for the FPGA end

SD Card Pin	FPGA Pin Name	Pin Position
SD-CLK	IO-22P-47	U26

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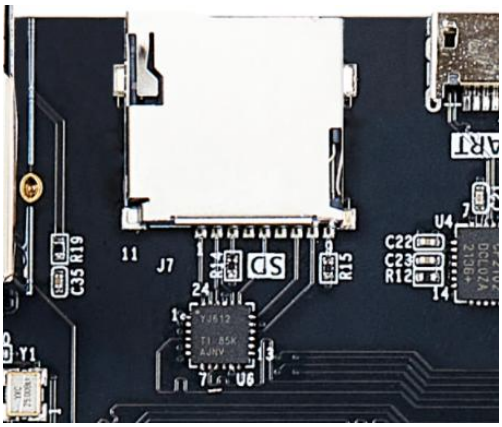
SD-CMD	IO-22N-47	U27
SD-DATA0	IO-1N-47	Y27
SD-DATA1	IO-1P-47	Y26
SD-DATA2	IO-19N-47	V28
SD-DATA3	IO-19P-47	V27

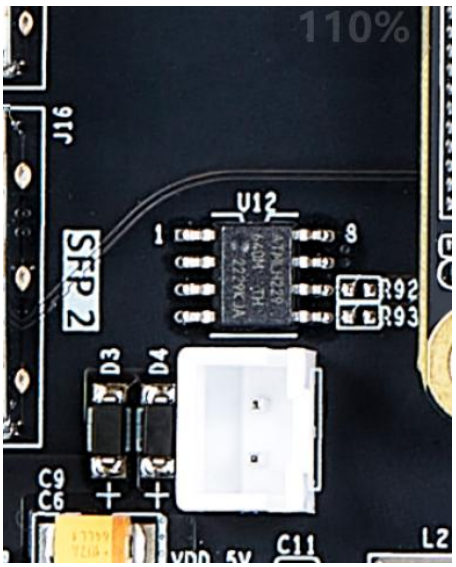


Part 4.5: E2PROM

A 64Kbit EEPROM chip, AT24C64D-SSHM-T, is placed on the FPGA Carrier board, which is connected to BANK65 of FPGA through IIC bus. The read address of EEPROM is 0xA1 and the write address is 0xA0.

The following is the pin assignment and schematic diagram of EEPROM.

EEPROM Pin	FPGA Pin Name	Pin Position
IIC-CLK	IO-12P-MRCC-65	N24
IIC-DATA	IO-12N-MRCC-65	M24



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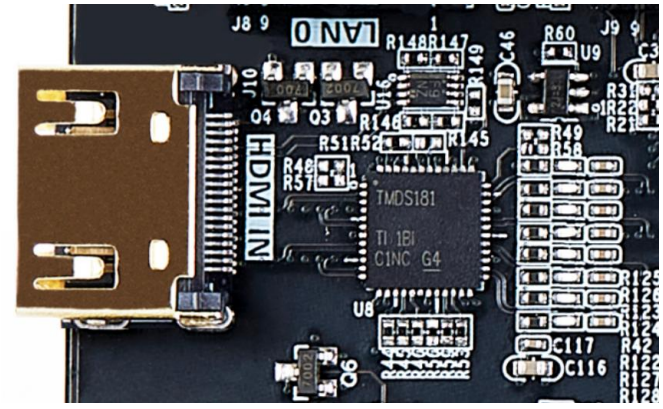
Part 4.6: HDMI Input (4K 60FPS)

The FPGA development board is designed with HDMI input interface, which can realize 4K/60FPS image input with multiple resolutions and adjustable frame rates.

The following table lists the pin correspondences, detailed circuitry can refer to the development board schematic.

HDMI Input	MPSOC Pin Name	Pin Position
GTX_HDMI_IN_P0	MGT_RX_P0_224	AP2
GTX_HDMI_IN_N0	MGT_RX_N0_224	AP1
GTX_HDMI_IN_P1	MGT_RX_P1_224	AM2
GTX_HDMI_IN_N1	MGT_RX_N1_224	AM1
GTX_HDMI_IN_P2	MGT_RX_P2_224	AK2
GTX_HDMI_IN_N2	MGT_RX_N2_224	AK1
GTX_HDMI_IN_CLK_P	MGT_CLK1_P_224	AF6
GTX_HDMI_IN_CLK_N	MGT_CLK1_N_224	AF5
F_HDMI_IN_HPD	IO_L17N_64	AD8
F_HDMI_SCL_CTL	IO_L14P_64	AF9
F_HDMI_SDA_CTL	IO_L14N_64	AG9
HDMI_IN_PWR_DET	IO_L22N_64	AP8
F_HDMI_IN_I2C_SCL	IO_L24P_64	AK8
F_HDMI_IN_I2C_SDA	IO_L24N_64	AL8



Part 4.7: HDMI Output (4K 60FPS)

The FPGA development board is designed with HDMI output interface, which can achieve 4K/60FPS image output with multiple resolutions and adjustable frame rates.

The following table lists the pin correspondences, detailed circuitry can refer to the development board schematic.

HDMI Input	MPSOC Pin Name	Pin Position
GTX_HDMI_OUT_P0	MGT_TX_P0_224	AN4
GTX_HDMI_OUT_N0	MGT_TX_N0_224	AN3

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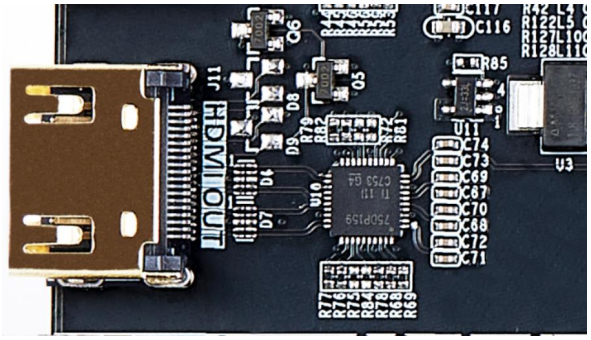
GTX_HDMI_OUT_P1	MGT_TX_P1_224	AM6
GTX_HDMI_OUT_N1	MGT_TX_N1_224	AM5
GTX_HDMI_OUT_P2	MGT_TX_P2_224	AL4
GTX_HDMI_OUT_N2	MGT_TX_N2_224	AL3
GTX_HDMI_CLK_P	GTX_HDMI_CLK_P1	AD6
GTX_HDMI_CLK_N	GTX_HDMI_CLK_N1	AD5
GTX_HDMI_OUT_CLK_P	IO_L20P_47	U24
GTX_HDMI_OUT_CLK_N	IO_L20N_47	U25
F_HDMI_OUT_HPD	IO_L17P_64	AD9
F_HDMI_OUT_SCL_SRC	IO_L18P_64	AH9
F_HDMI_OUT_SDA_SRC	IO_L18N_64	AH8
F_HDMI_SCL_CTL	IO_L14P_64	AF9
F_HDMI_SDA_CTL	IO_L14N_64	AG9
F_HDMI_OUT_OE	IO_L15P_64	AE8
F_HDMI_OUT_CEC	IO_L15N_64	AF8



Part 4.8: Gigabit Ethernet

Two Gigabit Ethernet chips are placed on the FPGA development board. One has been integrated into the core board and the other is placed on the carrier board. The Ethernet chip and the FPGA chip are interconnected through the RGMII interface. Refer to the following table for connecting the corresponding pins.

Chip address PHY_AD[2:0]=001 on core board and PHY_AD[2:0]=010 on FPGA development board. The connection schematic can be referred to the following diagram (ESD protection circuit is required for the product circuit).

Gigabit Ethernet 1			Gigabit Ethernet 2		
RMGII Signal	FPGA Pin Name	Pin Position	RMGII Signal	FPGA Pin Name	Pin Position
TX_CLK	IO_14P_MRCC_65	P24	TX_CLK	IO_21P_47	W28
TXD0	IO_15P_65	T27	TXD0	IO_23P_47	V29
TXD1	IO_15N_65	R27	TXD1	IO_23N_47	W29
TXD2	IO_16P_65	T24	TXD2	IO_24P_47	V26
TXD3	IO_16N_65	T25	TXD3	IO_24N_47	W26
TX_EN	IO_17P_65	R25	TX_EN	IO_21N_47	Y28

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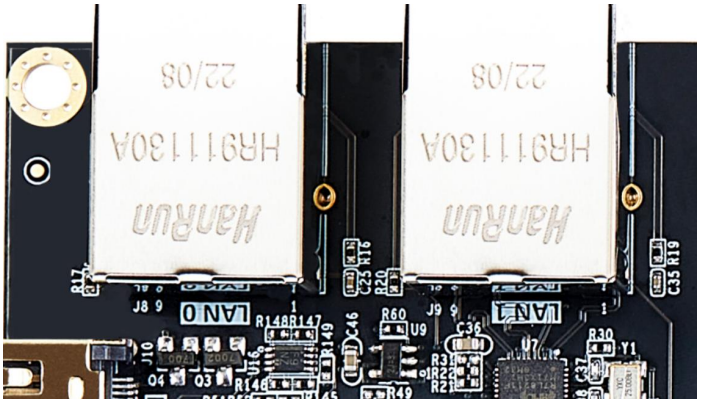
RX_CLK	IO_13P_MRCC_65	P26	RX_CLK	IO_13P_MRCC_47	W23
RXD0	IO_17N_65	R26	RXD0	IO_13N_MRCC_4	W24
RXD1	IO_18P_65	R23	RXD1	IO_17P_47	T22
RXD2	IO_18N_65	P23	RXD2	IO_17N_47	T23
RXD3	IO_19P_65	N22	RXD3	IO_16P_47	V22
RX_CTL	IO_19N_65	M22	RX_DV	IO_16N_47	V23
PHY_nRST	IO_13N_SRCC_65	N26	MDC	IO_15P_47	U21
MDC	IO_20P_65	P20	MDIO	IO_15N_47	U22



Part 4.9: SFP

Two SFP interfaces are designed on the FPGA development board, the interface signals are connected to the BANK228 of the FPGA, please refer to the schematic for details. The following is the pin assignment of the SFP, the schematic can be viewed under the folder.

SFP1 Pin	FPGA Pin Name	Pin Position
SFP-TX-P1	MGT-TX-P2-228	C4
SFP-TX-N1	MGT-TX-N2-228	C3
SFP-RX-P1	MGT-RX-P2-228	B2
SFP-RX-N1	MGT-RX-N2-228	B1

SFP2 Pin	FPGA Pin Name	Pin Position
SFP-TX-P2	MGT-TX-P3-118	B6
SFP-TX-N2	MGT-TX-N3-118	B5
SFP-RX-P2	MGT-RX-P3-118	A4
SFP-RX-N2	MGT-RX-N3-118	A3

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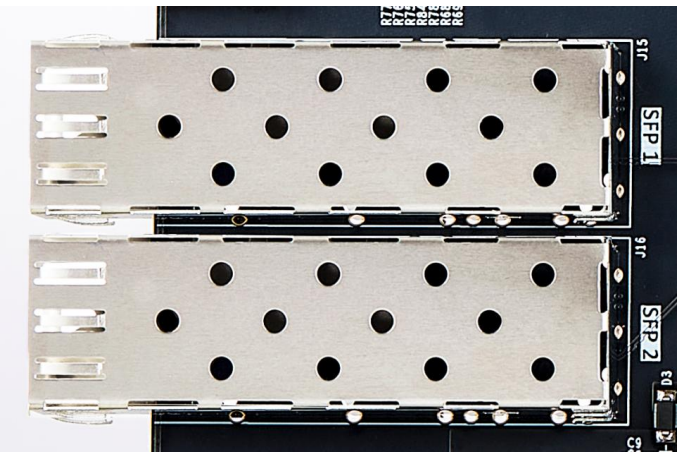
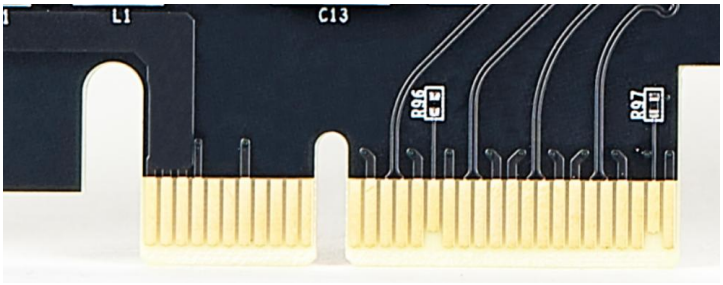


Part 4.10: PCIE3.0 Interface

The PCIE3.0 x4 interface is designed on FPGA the development board, and the interface signals are connected to the BANK65/BANK227 of the FPGA, please refer to the schematic for details.

PCIE3.0 Interface	MPSOC Pin Name	Pin Position
PERST_N	IO_PERSTN0_65	K22
REF_CLK_P	MGT_CLK_P0_227	P6
REF_CLK_N	MGT_CLK_N0_227	P5
PER0_P	MGT_TX_P3_227	G4
PER0_N	MGT_TX_N3_227	G3
PER1_P	MGT_TX_P2_227	J4
PER1_N	MGT_TX_N2_227	J3
PER2_P	MGT_TX_P1_227	L4
PER2_N	MGT_TX_N1_227	L3
PER3_P	MGT_TX_P0_227	N4
PER3_N	MGT_TX_N0_227	N3
PET0_P	MGT_RX_P3_227	F2
PET0_N	MGT_RX_N3_227	F1
PET1_P	MGT_RX_P2_227	H2
PET1_N	MGT_RX_N2_227	H1
PET2_P	MGT_RX_P1_227	K2
PET2_N	MGT_RX_N1_227	K1
PET3_P	MGT_RX_P0_227	M2
PET3_N	MGT_RX_N0_227	M1



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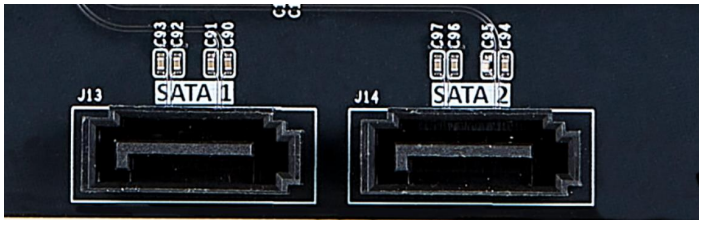
Part 4.11: SATA Interface

The FPGA development board has a reserved SATA interface, which is connected to the BANK228 of the FPGA, please refer to the schematic for details. This interface is only reserved, not open routines.

Signal Sequence	FPGA Pin Name	Pin Location
SATA1-TX-P	MGT_TX_P1_228	D6
SATA1-TX-N	MGT_TX_N1_228	D5
SATA1-RX-P	MGT_RX_P1_228	D2
SATA1-RX-N	MGT_RX_N1_228	D1

Signal Sequence	FPGA Pin Name	Pin Location
SATA2-TX-P	MGT_TX_P0_228	F6
SATA2-TX-N	MGT_TX_N0_228	F5
SATA2-RX-P	MGT_RX_P0_228	E4
SATA2-RX-N	MGT_RX_N0_228	E3



Part 4.12: 40P Expansion Ports

The FPGA development board has a 40P 0.1 inch simple bullhorn holder on board for expansion signal connection. The level of the BANK64 part is 3.3V. The following table shows the location of the chip where the signals are located, refer to the schematic section for detailed connections.

JM1 Signal	FPGA Pin Name	Pin Position	JM1 Signal	FPGA Pin Name	Pin Position
5	**IO_L2P_64**	**AN13**	**6**	**IO_L8P_64**	**AH13**
7	IO_L2N_64	AP13	8	IO_L8N_64	AJ13
9	IO_L6P_64	AK13	10	IO_L11P_SRCC_64	AG12
11	IO_L6N_64	AL13	12	IO_L11N_SRCC_64	AH12
13	IO_L4P_64	AM12	14	IO_L7P_64	AE13
15	IO_L4N_64	AN12	16	IO_L7N_64	AF13
17	IO_L5P_64	AK12	18	IO_L9P_64	AE12
19	IO_L5N_64	AL12	20	IO_L9N_64	AF12
21	IO_L3P_64	AM11	22	IO_L12P_MRCC_64	AG11
23	IO_L3N_64	AN11	24	IO_L12N_MRCC_64	AH11
25	IO_L21P_64	AK10	26	IO_L10P_64	AD11
27	IO_L21N_64	AL9	28	IO_L10N_64	AE11
29	IO_L1P_64	AP11	30	IO_L13P_MRCC_64	AF10

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31	IO_L1N_64	AP10	32	IO_L13N_MRCC_64	AG10
37	IO_L19P_64	AL10	38	IO_L16P_64	AD10
39	IO_L19N_64	AM10	40	IO_L16N_64	AE10



Part 4.13: 120P Expansion Ports

The FPGA development board has a 120P 0.6mm pitch simple bullhorn holder on board for expansion signal connection. The level of the BANK45 part can be adjusted to 1.8/2.5/3.3V. The following table shows the location of the chip where the signals are located, refer to the schematic section for detailed connections.

J9 Signal	FPGA Pin Name	Pin Position	J9 Signal	FPGA Pin Name	Pin Position
9	IO_L2P_45	AN19	10	IO_L17P_45	AG19
11	IO_L2N_45	AP18	12	IO_L17N_45	AH19
15	IO_L8P_45	AL19	16	IO_L19P_45	AD19
17	IO_L8N_45	AM19	18	IO_L19N_45	AD18
21	IO_L10P_45	AL18	22	IO_L13P_MRCC _45	AH18
23	IO_L10N_45	AL17	24	IO_L13N_MRCC _45	AH17
27	IO_L4P_45	AN18	28	IO_L21P_45	AE18
29	IO_L4N_45	AN17	30	IO_L21N_45	AF18
33	IO_L3P_45	AM17	34	IO_L24P_45	AD16
35	IO_L3N_45	AN16	36	IO_L24N_45	AD15
39	IO_L9P_45	AK15	40	IO_L23P_45	AE17
41	IO_L9N_45	AL15	42	IO_L23N_45	AF17
45	IO_L6P_45	AP16	46	IO_L15P_45	AG17
47	IO_L6N_45	AP15	48	IO_L15N_45	AG16
51	IO_L5P_45	AM16	52	IO_L18P_45	AG15
53	IO_L5N_45	AM15	54	IO_L18N_45	AG14
57	IO_L11P_MRCC_45	AJ18	58	IO_L22P_45	AE16
59	IO_L11N_MRCC _45	AK18	60	IO_L22N_45	AE15
63	IO_L1P_45	AN14	64	IO_L14P_MRCC _45	AH16
65	IO_L1N_45	AP14	66	IO_L14N_MRCC _45	AJ16
69	IO_L12P_MRCC _45	AK17	70	IO_L16P_45	AJ15
71	IO_L12N_MRCC _45	AK16	72	IO_L16N_45	AJ14
75	IO_L7P_45	AL14	76	IO_L20P_45	AF15
77	IO_L7N_45	AM14	78	IO_L20N_45	AF14

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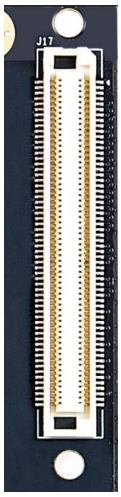

Part 4.14: FMC HPC Expansion Ports

One way FMC HPC connector is designed on the FPGA development board, and the following table lists the signal correspondences. Refer to the schematic section for detailed connections.

FMC HPC Pin	MPSOC Pin Name	Pin Position
LA00_P_CC	IO_L13P_MRCC_44	AJ21
LA00_N_CC	IO_ L13N_MRCC _44	AK21
LA01_P_CC	IO_L14P_MRCC_44	AK22
LA01_N_CC	IO_ L14N_MRCC _44	AK23
LA02_P	IO_L16P_44	AJ20
LA02_N	IO_L16N_44	AK20
LA03_P	IO_L15P_44	AL20
LA03_N	IO_L15N_44	AM20
LA04_P	IO_L3P_44	AD20
LA04_N	IO_L3N_44	AE20
LA05_P	IO_L17P_44	AL22
LA05_N	IO_L17N_44	AL23
LA06_P	IO_L22P_44	AP20
LA06_N	IO_L22N_44	AP21
LA07_P	IO_L20P_44	AM22
LA07_N	IO_L20N_44	AN22
LA08_P	IO_L19P_44	AM21
LA08_N	IO_L19N_44	AN21
LA09_P	IO_L21P_44	AM24
LA09_N	IO_L21N_44	AN24
LA10_P	IO_L24P_44	AN23
LA10_N	IO_L24N_44	AP23
LA11_P	IO_L7P_44	AE25
LA11_N	IO_L7N_44	AE26
LA12_P	IO_L23P_44	AP24

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LA12_N	IO_L23N_44	AP25
LA13_P	IO_L8P_44	AF23
LA13_N	IO_L8N_44	AF24
LA14_P	IO_L10P_44	AH24
LA14_N	IO_L10N_44	AJ25
LA15_P	IO_L9P_44	AG24
LA15_N	IO_L9N_44	AG25
LA16_P	IO_L18P_44	AL24
LA16_N	IO_L18N_44	AL25
LA17_P_CC	IO_L11P_SRCC_44	AJ23
LA17_N_CC	IO_L11N_SRCC_44	AJ24
LA18_P_CC	IO_L12P_MRCC_44	AH22
LA18_N_CC	IO_L12N_MRCC_44	AH23
LA19_P	IO_L4P_44	AG21
LA19_N	IO_L4N_44	AH21
LA20_P	IO_L6P_44	AF22
LA20_N	IO_L6N_44	AG22
LA21_P	IO_L7P_47	AA22
LA21_N	IO_L7N_47	AB22
LA22_P	IO_L10P_47	AB21
LA22_N	IO_L10N_47	AC21
LA23_P	IO_L5P_44	AE22
LA23_N	IO_L5N_44	AE23
LA24_P	IO_L9P_47	AA20
LA24_N	IO_L9N_47	AB20
LA25_P	IO_L3P_47	AB24
LA25_N	IO_L3N_47	AC24
LA26_P	IO_L2P_44	AF20
LA26_N	IO_L2N_44	AG20
LA27_P	IO_L1P_44	AD21
LA27_N	IO_L1N_44	AE21
LA28_P	IO_L6P_47	AB25
LA28_N	IO_L6N_47	AB26
LA29_P	IO_L8P_47	AC22
LA29_N	IO_L8N_47	AC23
LA30_P	IO_L4P_47	AC26
LA30_N	IO_L4N_47	AC27
LA31_P	IO_L2P_47	AD25
LA31_N	IO_L2N_47	AD26
LA32_P	IO_L5P_47	AA27
LA32_N	IO_L5N_47	AB27
LA33_P	IO_L18P_47	V21
LA33_N	IO_L18N_47	W21
FMC_IIC_SCL	IO_L12P_65	N24
FMC_IIC_SDA	IO_L12N_65	M24
DP0_M2C_P	MGT_RX_P2_225	AD2
DP0_M2C_N	MGT_RX_N2_225	AD1

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DP1_M2C_P	MGT_RX_P0_225	AH2
DP1_M2C_N	MGT_RX_N0_225	AH1
DP2_M2C_P	MGT_RX_P1_225	AF2
DP2_M2C_N	MGT_RX_N1_225	AF1
DP3_M2C_P	MGT_RX_P3_225	AB2
DP3_M2C_N	MGT_RX_N3_225	AB1
DP4_M2C_P	MGT_RX_P1_226	V2
DP4_M2C_N	MGT_RX_N1_226	V1
DP5_M2C_P	MGT_RX_P3_226	P2
DP5_M2C_N	MGT_RX_N3_226	P1
DP6_M2C_P	MGT_RX_P2_226	T2
DP6_M2C_N	MGT_RX_N2_226	T1
DP7_M2C_P	MGT_RX_P0_226	Y2
DP7_M2C_N	MGT_RX_N0_226	Y1
GBTCLK0_M2C_P	MGT_CLK0_P_225	AB6
GBTCLK0_M2C_N	MGT_CLK0_N_225	AB5
GBTCLK1_M2C_P	MGT_CLK0_P_226	V6
GBTCLK1_M2C_N	MGT_CLK0_N_226	V5
DP0_C2M_P	MGT_TX_P2_225	AE4
DP0_C2M_N	MGT_TX_N2_225	AE3
DP1_C2M_P	MGT_TX_P0_225	AH6
DP1_C2M_N	MGT_TX_N0_225	AH5
DP2_C2M_P	MGT_TX_P1_225	AG4
DP2_C2M_N	MGT_TX_N1_225	AG3
DP3_C2M_P	MGT_TX_P3_225	AC4
DP3_C2M_N	MGT_TX_N3_225	AC3
DP4_C2M_P	MGT_TX_P1_226	W4
DP4_C2M_N	MGT_TX_N1_226	W3
DP5_C2M_P	MGT_TX_P3_226	R4
DP5_C2M_N	MGT_TX_N3_226	R3
DP6_C2M_P	MGT_TX_P2_226	U4
DP6_C2M_N	MGT_TX_N2_226	U3
DP7_C2M_P	MGT_TX_P0_226	AA4
DP7_C2M_N	MGT_TX_N0_226	AA3
HA00_P_CC	IO_L11P_SRCC_46	AL29
HA00_N_CC	IO_L11N_SRCC_46	AM29
HA01_P_CC	IO_L13P_SRCC_46	AJ29
HA01_N_CC	IO_L13N_SRCC_46	AK30
HA02_P	IO_L15P_46	AJ30
HA02_N	IO_L15N_46	AJ31
HA03_P	IO_L5P_46	AH27
HA03_N	IO_L5N_46	AH28
HA04_P	IO_L9P_46	AN27
HA04_N	IO_L9N_46	AN28
HA05_P	IO_L10P_46	AN29
HA05_N	IO_L10N_46	AP30
HA06_P	IO_L22P_46	AN34

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HA06_N	IO_L22N_46	AP34
HA07_P	IO_L23P_46	AM32
HA07_N	IO_L23N_46	AN32
HA08_P	IO_L7P_46	AN26
HA08_N	IO_L7N_46	AP26
HA09_P	IO_L4P_46	AL27
HA09_N	IO_L4N_46	AL28
HA10_P	IO_L24P_46	AL34
HA10_N	IO_L24N_46	AM34
HA11_P	IO_L20P_46	AN33
HA11_N	IO_L20N_46	AP33
HA12_P	IO_L21P_46	AN31
HA12_N	IO_L21N_46	AP31
HA13_P	IO_L2P_46	AM26
HA13_N	IO_L2N_46	AM27
HA14_P	IO_L19P_46	AL32
HA14_N	IO_L19N_46	AL33
HA15_P	IO_L3P_46	AK26
HA15_N	IO_L3N_46	AK27
HA16_P	IO_L8P_46	AP28
HA16_N	IO_L8N_46	AP29
HA17_P_CC	IO_L14P_SRCC_46	AK31
HA17_N_CC	IO_L14N_SRCC_46	AK32
HA18_P_CC	IO_L12P_SRCC_46	AL30
HA18_N_CC	IO_L12N_SRCC_46	AM30
HA19_P	IO_L1P_46	AH26
HA19_N	IO_L1N_46	AJ26
HA20_P	IO_L6P_46	AJ28
HA20_N	IO_L6N_46	AK28
HA21_P	IO_L16P_46	AH33
HA21_N	IO_L16N_46	AJ33
HA22_P	IO_L17P_46	AH31
HA22_N	IO_L17N_46	AH32
HA23_P	IO_L18P_46	AH34
HA23_N	IO_L18N_46	AJ34
HB00_P_CC	IO_L11P_SRCC_48	AD30
HB00_N_CC	IO_L11N_SRCC_48	AD31
HB01_P_CC	IO_L2P_48	AE28
HB01_N_CC	IO_L2N_48	AF28
HB02_P	IO_L6P_48	AF30
HB02_N	IO_L6N_48	AG30
HB03_P	IO_L4P_48	AF29
HB03_N	IO_L4N_48	AG29
HB04_P	IO_L1P_48	AE27
HB04_N	IO_L1N_48	AF27
HB05_P	IO_L8P_48	AF33
HB05_N	IO_L8N_48	AG34

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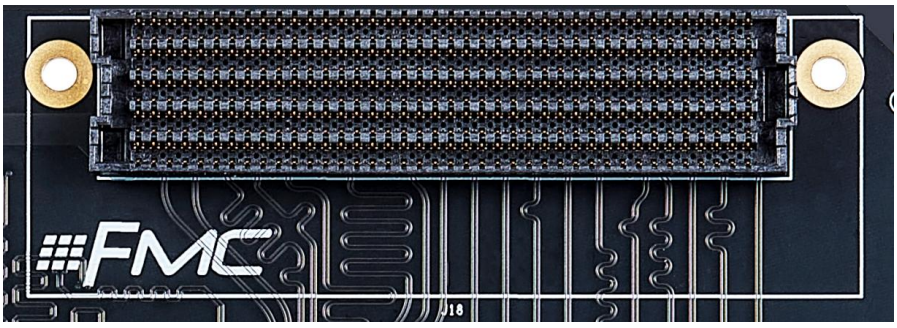
HB06_P	IO_L12P_SRCC_48	AC31
HB06_N	IO_L12N_SRCC_48	AC32
HB07_P	IO_L3P_48	AC28
HB07_N	IO_L3N_48	AD28
HB08_P	IO_L10P_48	AE33
HB08_N	IO_L10N_48	AF34
HB09_P	IO_L7P_48	AG31
HB09_N	IO_L7N_48	AG32
HB10_P	IO_L22P_48	Y31
HB10_N	IO_L22N_48	Y32
HB11_P	IO_L16P_48	AA29
HB11_N	IO_L16N_48	AB29
HB12_P	IO_L18P_48	AC33
HB12_N	IO_L18N_48	AD33
HB13_P	IO_L9P_48	AE32
HB13_N	IO_L9N_48	AF32
HB14_P	IO_L20P_48	W30
HB14_N	IO_L20N_48	Y30
HB15_P	IO_L19P_48	W33
HB15_N	IO_L19N_48	Y33
HB16_P	IO_L5P_48	AD29
HB16_N	IO_L5N_48	AE30
HB17_P_CC	IO_L14P_SRCC_48	AB30
HB17_N_CC	IO_L14N_SRCC_48	AB31
HB18_P_CC	IO_L24P_48	V31
HB18_N_CC	IO_L24N_48	W31
HB19_P	IO_L15P_48	AC34
HB19_N	IO_L15N_48	AD34
HB20_P	IO_L211P_48	V33
HB20_N	IO_L21N_48	W34
HB21_P	IO_L17P_48	AA34
HB21_N	IO_L17N_48	AB34



Part 4.15: LEDs

The core board is designed with five LEDs, and the development board is designed with two LEDs,

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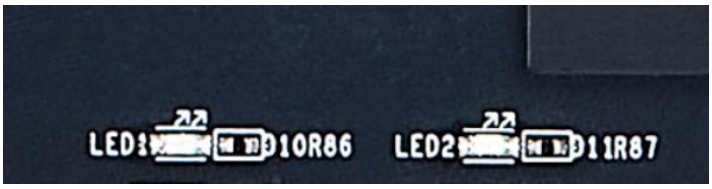
for a total of seven LEDs.The pin positions of the LEDs are shown in the table below.The LEDs light up when the pin outputs a high level, and the LEDs go out when the pin outputs a low level.

LED	FPGA Pin Name	Pin Position
LED1（SOM）	IO_T0U_65	H23
LED2（SOM）	IO_T2U_65	N27
LED3（SOM）	IO_23P_65	N21
LED4（SOM）	IO_23N_65	M21
LED5（SOM）	IO_2P_65	G25
LED1 (FPGA Development Board)	IO-L23N-64	AJ8
LED2 (FPGA Development Board)	IO-L22P-64	AN8



Part 4.16: KEYs

The FPGA development board is designed with two-way keys. The keys are high by default and low when pressed. The keys are connected to the PL side and can also be assigned to the ARM side through the EMIO method, and the pin positions of the keys are listed in the table below.

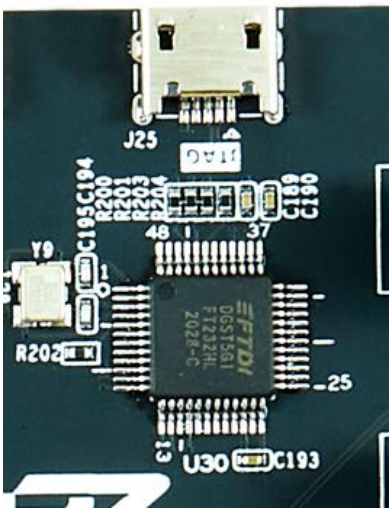
KEY Number	FPGA Pin Name	Pin Position
KEY 1	IO-L20P-64	AN9
KEY 2	IO-L20N-64	AP9



Part 4.17: USB to JTAG Downloader

FPGA development board has a USB to JTAG downloader on board, after installing the Vivado software, use the USB cable to connect the USB port corresponding to JTAG, you can achieve debugging and downloading, very convenient.

The following is the location of the interface on the development board.



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