Cruetech Kintex-7

Family Board

K7325T/K7410T SOM

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Part 1: SOM Introduction

Part 1.1: SOM Introduction

The CRK7325TC/410TC core board is equipped with a Xilinx KINTEX-7 FPGA chip, themodel is XC7K325T-2FFG900I/ XC7K410T-FFG900I. The FPGA chip package is FFG900, speed grade is -2, temperature grade is industrial grade.

The core board plugs into the carrier board connector through four 120P high-speed connectors, and the core board has four 3.5mm fixing holes placed on the four feet, which can be tightened with the carrier board by screws to ensure stable operation in a strong vibration environment.

Part 1.2: SOM Specification

CRK7325TC/CRK7410TC Industrial Grade SOM Specification		
FPGA	XC7K325T-2FFG900I	XC7K410T-2FFG900I
Logic Cells	326080	406720
Flip-Flops	407600	508400
Slices	50950	63550
DSP Slices	840	1540
Block RAM	445	795
DDR3/DD3L	2GB（Data Width 64bit)	
QSPI FLASH	32Mb, to store startup files and user files	
Start Method	JTAG/QSPI FLASH	
Gigabit Ethernet	1	
User LEDs	5 LEDs (High-level on, Low-level off)	
IO Number	288 IOs（ 1.8/2.5/3.3V adjustable, default by 3.3V)	
Number of GTX ports	4 BANK, 16 Paris of TX/RX each	
Working Voltage/Max. Current	5V/3A	
Working Temperature	-40°C~+85°C	
Form Factors	83.8mm x 64.8mm, Immersion Gold Process	
Technology	0.6mm 120P Connectors X 4	
Connectors Height	3mm	

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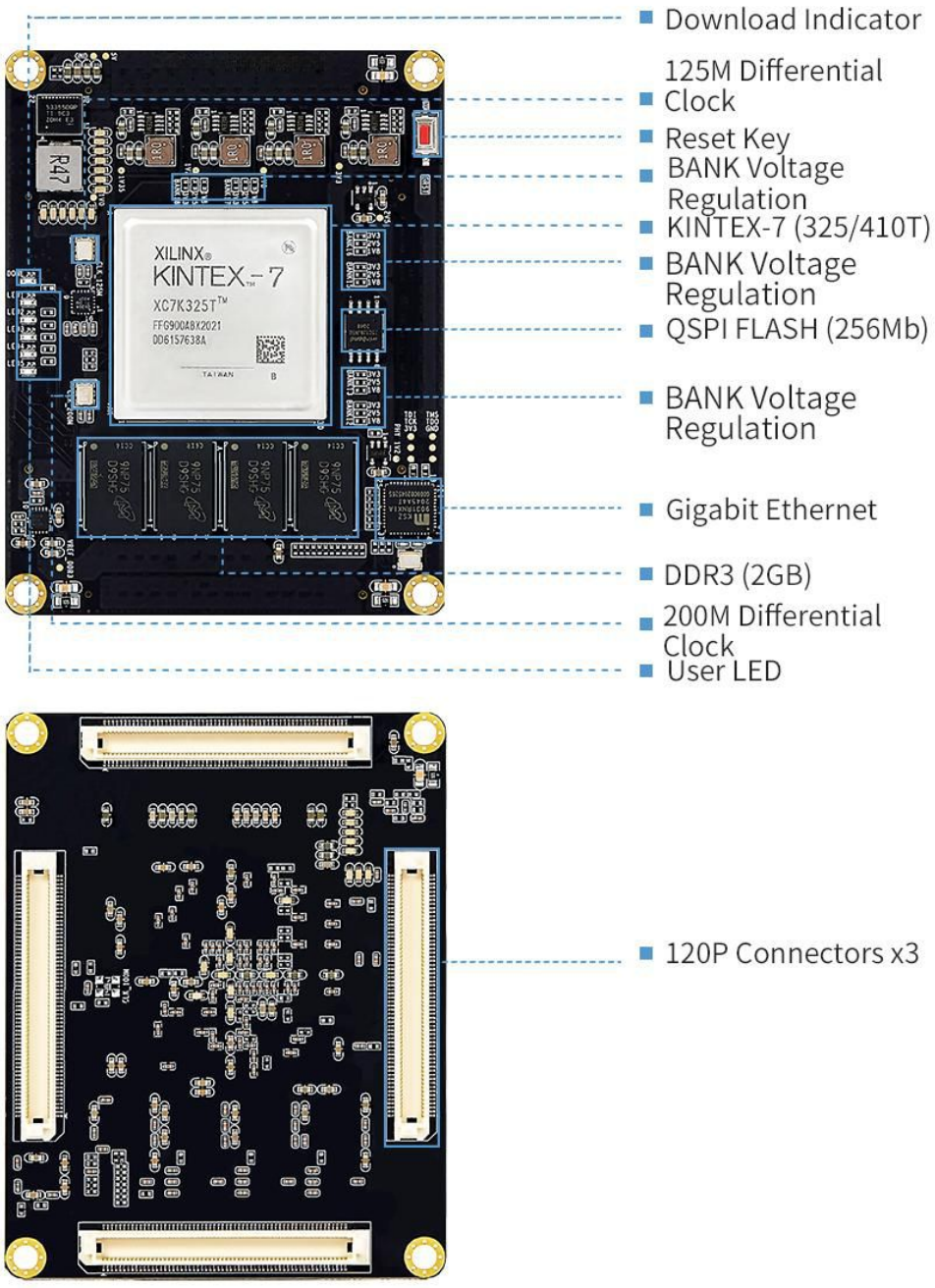
Part 1.3: Product Appearance

The following figure shows the location of each major electronic component on the core board for easy identification.



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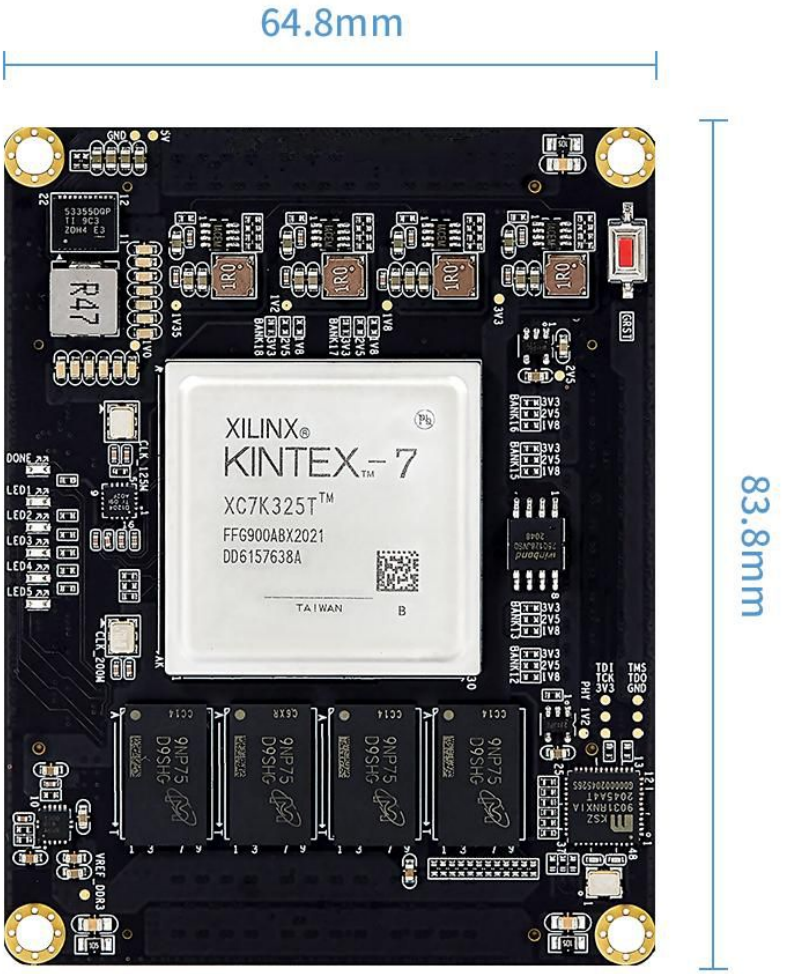
Part 1.4: SOM Form Factors

The core board size is 83.8 mm x 64.8mm. The core board is connected to the carrier board via four 0.6mm/120P gold-plated high-speed connectors on the bottom.





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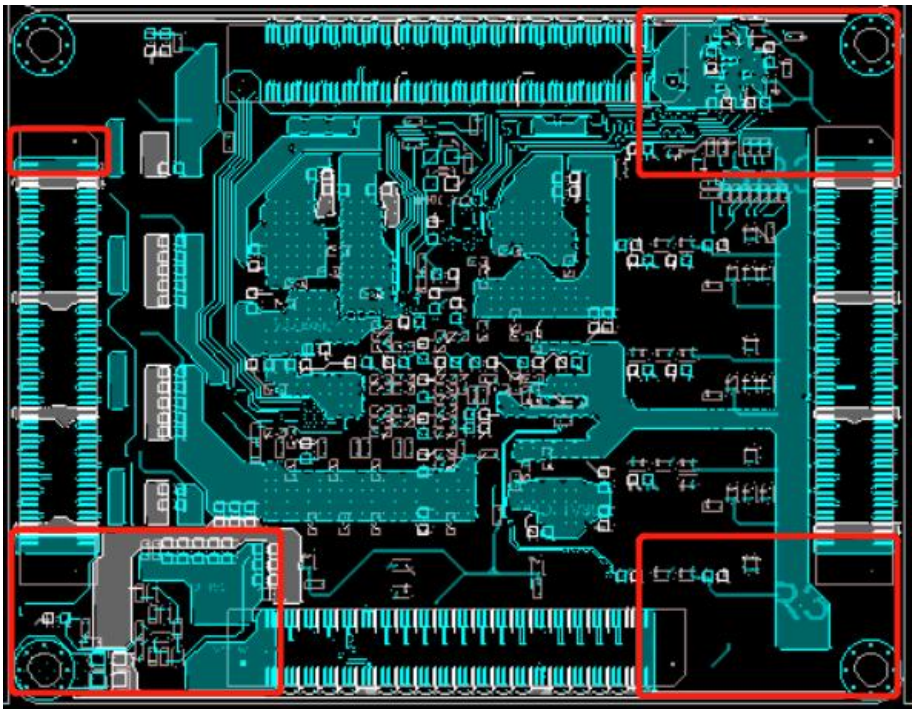
Part 2: SOM User Guide

Part 2.1: Power Connection

The power supply voltage range of the FPGA core board is 5V. The Power input pins are reserved at the four corners of the module, and the power pins have been connected inside the module. When designed, it only needs to connect the power pin core board at one corner to work. The power connection needs to be connected with copper and enough holes are made to ensure the power flow ability. All GND signals on the module need to be connected to the base plate, and each GND is connected to the carrier board through two through-holes to ensure through-flow capability. The limit current of the core board is 5V/3A, so the external power supply needs to consider the limit current situation to ensure the stable operation of the core board.

The power supply output voltage of the module power supply needs to be stable, in the module power supply input plus a level of DCDC power conversion, from high voltage to 5V, DCDC current output capacity can be selected about 5A, such as power chip MP2482 can be referenced. Two **220uF/ 10V** capacitors should be placed in the power input of the core board to ensure the quality of the power supply.



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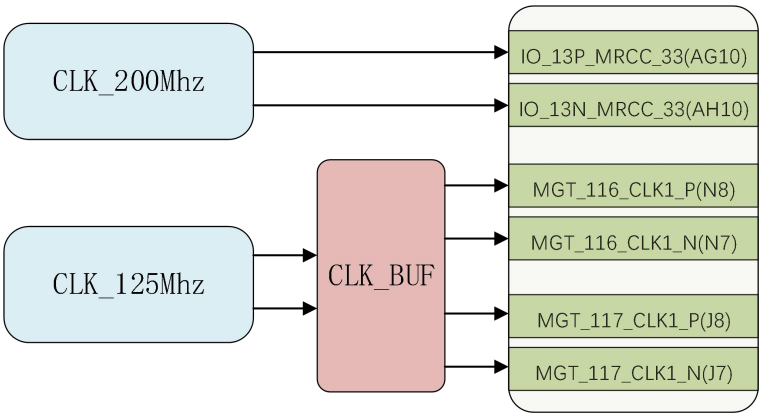
Part 2.2: Clock

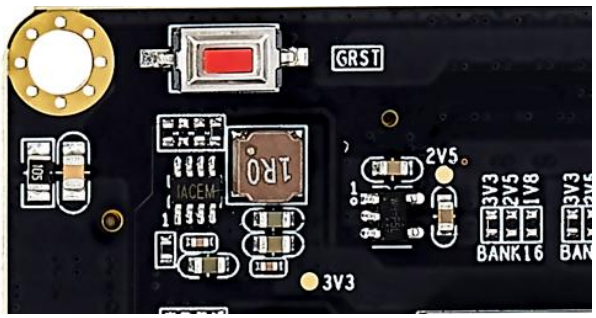
Two active differential crystals are placed on the core board, with a 200M clock providing a differential clock for the logic side and a 125M differential clock for the GTX interface. As shown in the figure below, the 200M differential clock is connected to the 13P/13N pin of BANK33, the corresponding pin position is AG10/AH10, and the 125M clock is converted into two N8/N7 and J8/J7 positions to BANK116/117 respectively



Part 2.3: Global Reset

The core board reserves a reset key for debugging use, this reset key uses RC circuitry, the reset is not sufficient, only used for debugging, the key is connected with the FPGA BANK14, the corresponding pin is "**IO_12P_MRCC_14 (T26)**". Actual products require a reset circuit, and a dedicated reset chip can be used on the carrier board, such as the **MAX811**, or other chips with a longer reset time.





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Part 2.4: Boot Mode Selection

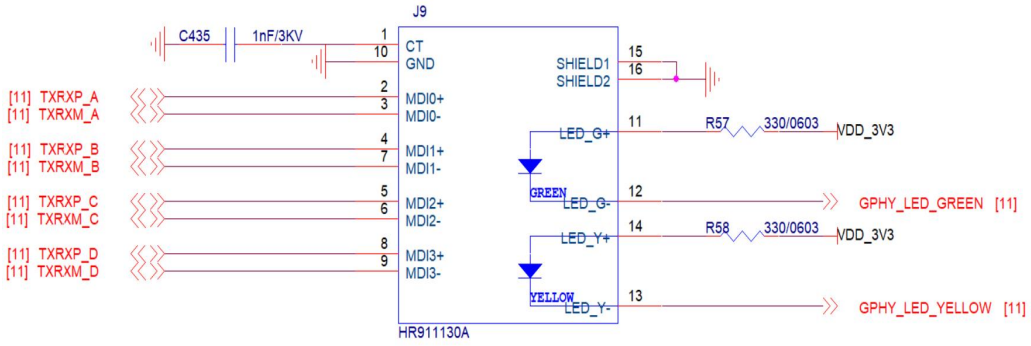
The core board supports two boot modes, namely JTAG and QSPI Flash. The default is QSPI Flash startup.

Part 2.5: Network Port Connection

A gigabit Ethernet chip KSZ9031 is placed on the core board, and the Ethernet chip and ZYNQ chip are connected through the RGMII interface. The corresponding pins are shown in the following table. For Ethernet external connection, only an RJ45 with transformer is required, and the chip address is PHY_AD[2:0]=001. The connection schematic diagram can refer to the following figure (the product circuit needs to add an ESD protection circuit).

Note: The product circuit needs to add electrostatic protection on the network port signal line and LED, and the 0.1uF capacitor should be 2KV or 3KV withstanding voltage.

RMGII Signal	Pin Name	Pin Position
TX_CLK	IO_13N_MRCC_14	U28
TXD0	IO_14P_MRCC_14	T25
TXD1	IO_14N_MRCC_14	U25
TXD2	IO_15P_14	U29
TXD3	IO_15N_14	U30
TX_EN	IO_16P_14	V26
RX_CLK	IO_13P_MRCC_14	U27
RXD0	IO_16N_14	V27
RXD1	IO_17P_14	V29
RXD2	IO_17N_14	V30
RXD3	IO_18P_14	V25
RX_CTL	IO_18N_14	W26
PHY_nRST (Power on Reset by Default)	IO_20P_14	W23
MDC	IO_19P_14	V19
MDIO	IO_19N_14	V20



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Part 2.6: QSPI FLASH

The onboard 32MB QSPI FLASH, the model is MX25L25645GM2I-08G, is used to store the boot file.

QSPI FLASH Pin	Pin Name	Pin Position
DATA0	IO_1P_14	P24
DATA1	IO_1N_14	R25
DATA2	IO_2P_14	R20
DATA3	IO_2N_14	R21
QSPI_CS	IO_6P_14	R23
QSPI_CLK	CCLK_0	B10

Part 2.7: On-board LED

In order to facilitate debugging, five LEDs are placed on the core board. The pin positions of the LEDs are as shown in the table below. When the pin outputs a high level, the LED lights up, and when the pin outputs a high level, the LED turns off.

LED Pin	Pin Name	Pin Position
LED1	IO_23P_14	U24
LED2	IO_23N_14	V24
LED3	IO_24P_14	W21
LED4	IO_24N_14	W22
LED5	IO_25_14	W19

Part 2.8: BANK Interface Level Selection

The external banks on the core board are BANK12/13/14/15/32/33/34. The IOs of these banks can independently support three levels of 1.8V/2.5V/3.3V. The default level of BANK is 3.3V. If you need to change the level, you only need to replace the corresponding position resistor to realize the adjustment. The core board has marked the position of the BANK level adjustment resistor, as shown in the figure below.

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Part 2.9: DDR3

The PS side is equipped with four industrial-grade DDR3L chips, with a single capacity of 512MB and a total capacity of 2GB. The model is "**MT41K256M16TW-107IT:P**". DDR3L pin allocation refer to the following table.

DDR3L Pin	Pin Name	Pin Position
DDR3_D0	IO-L4N-32	AG14
DDR3_D1	IO-L5P-32	AH17
DDR3_D2	IO-L1N-32	AK15
DDR3_D3	IO-L4P-32	AF15
DDR3_D4	IO-L1P-32	AK16
DDR3_D5	IO-L6P-32	AE16
DDR3_D6	IO-L2N-32	AH15
DDR3_D7	IO-L5N-32	AJ17
DDR3_DM0	IO-L2P-32	AG15
DDR3_DQS_P0	IO-L3P-32	AH16
DDR3_DQS_N0	IO-L3N-32	AJ16

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DDR3_D8	IO-L8N-32	AH19
DDR3_D9	IO-L7N-32	AK19
DDR3_D10	IO-L10P-32	AD19
DDR3_D11	IO-L10N-32	AE19
DDR3_D12	IO-L11P-32	AF18
DDR3_D13	IO-L12N-32	AG17
DDR3_D14	IO-L8P-32	AG19
DDR3_D15	IO-L11N-32	AG18
DDR3_DM1	IO-L12P-32	AF17
DDR3_DQS_P1	IO-L9P-32	AJ18
DDR3_DQS_N1	IO-L9N-32	AK18
DDR3_D16	IO-L17N-32	AC19
DDR3_D17	IO-L18P-32	AB17
DDR3_D18	IO-L18N-32	AC17
DDR3_D19	IO-L16P-32	AA18
DDR3_D20	IO-L14P-32	AD17
DDR3_D21	IO-L16N-32	AB18
DDR3_D22	IO-L13N-32	AE18
DDR3_D23	IO-L17P-32	AB19
DDR3_DM2	IO-L14N-32	AD16
DDR3_DQS_P2	IO-L15P-32	Y19
DDR3_DQS_N2	IO-L15N-32	Y18
DDR3_D24	IO-L20N-32	AB15
DDR3_D25	IO-L23P-32	AA17
DDR3_D26	IO-L24N-32	Y15
DDR3_D27	IO-L19P-32	AE15
DDR3_D28	IO-L20P-32	AA15
DDR3_D29	IO-L22N-32	AD14
DDR3_D30	IO-L24P-32	Y16
DDR3_D31	IO-L22P-32	AC14
DDR3_DM3	IO-L23N-32	AA16
DDR3_DQS_P3	IO-L21P-32	AC16
DDR3_DQS_N3	IO-L21N-32	AC15
DDR3_D32	IO-L6P-34	AC7
DDR3_D33	IO-L1P-34	AD4
DDR3_D34	IO-L4N-34	AC4
DDR3_D35	IO-L5N-34	AE6
DDR3_D36	IO-L4P-34	AC5
DDR3_D37	IO-L5P-34	AD6
DDR3_D38	IO-L2N-34	AC1
DDR3_D39	IO-L1N-34	AD3

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DDR3_DM4	IO-L2P-34	AC2
DDR3_DQS_P4	IO-L3P-34	AD2
DDR3_DQS_N4	IO-L3N-34	AD1
DDR3_D40	IO-L7N-34	AF2
DDR3_D41	IO-L7P-34	AF3
DDR3_D42	IO-L11N-34	AF5
DDR3_D43	IO-L8P-34	AE1
DDR3_D44	IO-L11P-34	AE5
DDR3_D45	IO-L10N-34	AE3
DDR3_D46	IO-L12P-34	AF6
DDR3_D47	IO-L10P-34	AE4
DDR3_DM5	IO-L8N-34	AF1
DDR3_DQS_P5	IO-L9P-34	AG4
DDR3_DQS_N5	IO-L9N-34	AG3
DDR3_D48	IO-L16P-34	AH2
DDR3_D49	IO-L13N-34	AJ4
DDR3_D50	IO-L16N-34	AJ2
DDR3_D51	IO-L13P-34	AH4
DDR3_D52	IO-L17N-34	AK1
DDR3_D53	IO-L14P-34	AH6
DDR3_D54	IO-L17P-34	AJ1
DDR3_D55	IO-L18P-34	AJ3
DDR3_DM6	IO-L14N-34	AH5
DDR3_DQS_P6	IO-L15P-34	AG2
DDR3_DQS_N6	IO-L15N-34	AH1
DDR3_D56	IO-L23N-34	AK8
DDR3_D57	IO-L22N-34	AK6
DDR3_D58	IO-L23P-34	AJ8
DDR3_D59	IO-L24N-34	AK4
DDR3_D60	IO-L20P-34	AF7
DDR3_D61	IO-L24P-34	AK5
DDR3_D62	IO-L19P-34	AF8
DDR3_D63	IO-L22P-34	AJ6
DDR3_DM7	IO-L20N-34	AG7
DDR3_DQS_P7	IO-L21P-34	AH7
DDR3_DQS_N7	IO-L21N-34	AJ7
DDR3_A0	IO-L18P-33	AH11
DDR3_A1	IO-L21P-33	AH14
DDR3_A2	IO-L7N-33	AC10
DDR3_A3	IO-L10N-33	AE9
DDR3_A4	IO-L15N-33	AK9

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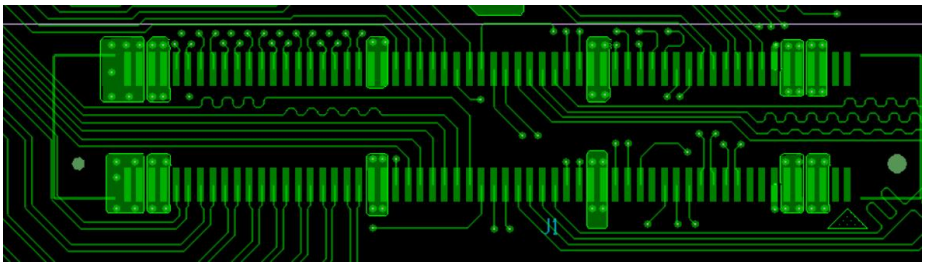
DDR3_A5	IO-L8N-33	AE8
DDR3_A6	IO-L19P-33	AE13
DDR3_A7	IO-L10P-33	AD9
DDR3_A8	IO-L23P-33	AF12
DDR3_A9	IO-L9P-33	AC12
DDR3_A10	IO-L18N-33	AJ11
DDR3_A11	IO-L20N-33	AK13
DDR3_A12	IO-L14P-33	AE10
DDR3_A13	IO-L7P-33	AB10
DDR3_A14	IO-L22N-33	AJ12
DDR3_BA0	IO-L22P-33	AJ13
DDR3_BA1	IO-L21N-33	AJ14
DDR3_BA2	IO-L9N-33	AC11
DDR3_CS	IO-L16P-33	AG9
DDR3_RAS	IO-L14N-33	AF10
DDR3_CAS	IO-L17P-33	AK11
DDR3_WE	IO-L16N-33	AH9
DDR3_ODT	IO-L20P-33	AK14
DDR3_RESET	IO-L8P-33	AD8
DDR3_CLK_P	IO-L12P-33	AD12
DDR3_CLK_N	IO-L12N-33	AD11
DDR3_CKE	IO-L17N-33	AK10

Part 3: Carrier Board Design

Part 3.1: PCB Design of Power Supply

The power input needs to be connected with copper skin, and enough via holes are made to ensure the current carrying capacity, but the power supply voltage is high and the interference is large. Under the condition of ensuring the current flow, do not make the copper skin larger, so as not to interfere with other signals. The ground pins need to be connected to the ground plane, and one ground pin needs to be punched with two vias to ensure flow and sufficient connection.



Part 3.2: High-speed interface layout and routing

1) Gigabit Ethernet:

The signal connected to the RJ45 end needs to keep the same length, and the TX part and the RX part of the RGMII interface need to keep the same length separately.

2) HDMI Interface

The HDMI interface signal needs to be differential, and the same length control must be maintained between the differentials.

3) Other high-speed interfaces

Control according to the interface specification

Part 3.3: LVDS Signal

The BANK of the module can be selected between three levels of 1.8V/2.5V/3.3V, the default is 3.3V level, if you need to work in LVDS mode, you need to adjust the interface level to 1.8V or 2.5V . At the same time, the LVDS signal traces need to be differentially processed, and the differentials must be of equal length.

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Part 3.4: LVDS Signal

There are many issues that need to be considered in GTX wiring. For users who have questions, they can contact customer service to access technical support.

Part 3.5: Product Protection

For product design, it is necessary to add protective circuits to various interfaces.It needs to be designed according to the requirements of the protection level

Part 4: Core Board Pins and Signal Equal Length

Part 4.1: SOM Core Board Pin Definition

The CRK7325TC/CRK7410TC core board pin definition We provide an explanatory document, please refer to the folder "CRK7325TC-410TC Core Board Pins and Equal Lengths".

Part 4.2: Signal Isometric

In order to facilitate the design of the carrier board and signal to go at high speed, we strictly make an equal length trace, and provide the trace length data on the J1-J4 connector. For a detailed data table, please refer to the folder "CRK7325TC-410TC Core Board Pins and Equal Lengths".

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