Kintex-7 Family Board

K7325T-FH/K7410T-FH User Manual



Version Records:

Data	Version	Description
2021.01.08	V1.1	initial version

This tutorial will continue to revise, optimize and increase based on the actual Experience, that is to provide you with more and better Demos.

If you find some errors or any suggestion, contact with us.

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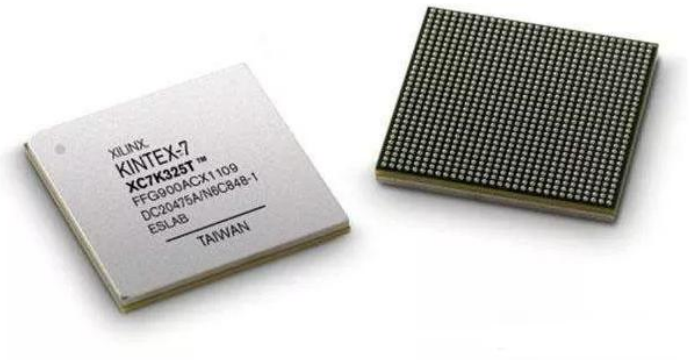
Par1: Kintex-7 series Introduction

The **Kintex-7** family is a new **Xilinx FPGA** that delivers comparable performance at less than half the price of the **Virtex-6** family, with twice the price/performance and half the power consumption.

This series not only provides the high-performance 10.3Gbps or low-cost optimized 6.5Gbps serial connectivity, memory and logic performance required for various applications such as high-volume 10G optical wired communication equipment. It also achieves the best balance of signal processing performance, power consumption and cost to support Long Term Evolution (LTE) wireless network deployments, meet the stringent power and cost requirements of next-generation high-definition 3D flat-panel displays, and deliver next-generation broadcast video-on-demand



Kintex-7 FPGAs

			Optimized for Best Price-Performance (1.0V, 0.95V, 0.9V)						
	Part Number		XC7K70T	XC7K160T	XC7K325T	XC7K355T	XC7K410T	XC7K420T	XC7K480T
	EasyPath™ Cost Reduction Solutions[1]		–	–	XCE7K325T	XCE7K355T	XCE7K410T	XCE7K420T	XCE7K480T
Logic Resources	Slices		10,250	25,350	50,950	55,650	63,550	65,150	74,650
	Logic Cells		65,600	162,240	326,080	356,160	406,720	416,960	477,760
	CLB Flip-Flops		82,000	202,800	407,600	445,200	508,400	521,200	597,200
Memory Resources	Maximum Distributed RAM (Kb)		838	2,188	4,000	5,088	5,663	5,938	6,788
	Block RAM/FIFO w/ ECC (36 Kb each)		135	325	445	715	795	835	955
	Total Block RAM (Kb)		4,860	11,700	16,020	25,740	28,620	30,060	34,380
Clock Resources	CMTs (1 MMCM + 1 PLL)		6	8	10	6	10	8	8
I/O Resources	Maximum Single-Ended I/O		300	400	500	300	500	400	400
	Maximum Differential I/O Pairs		144	192	240	144	240	192	192
Integrated IP Resources	DSP48 Slices		240	600	840	1,440	1,540	1,680	1,920
	PCIe® Gen2[2]		1	1	1	1	1	1	1
	Analog Mixed Signal (AMS) / XADC		1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks		1	1	1	1	1	1	1
	GTX Transceivers (12.5 Gb/s Max Rate)		8	8	16	24	16	32	32
Speed Grades	Commercial Temp (C)		-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Extended Temp (E)		-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3
	Industrial Temp (I)		-1, -2	-1, -2, -2L	-1, -2, -2L	-1, -2, -2L	-1, -2, -2L	-1, -2, -2L	-1, -2, -2L
	Package[3]	Dimensions (mm)	Available User I/O: 3.3V HR I/O, 1.8V HP I/Os (GTX)						
	FBG484[4]	23 x 23	185, 100 (4)	185, 100 (4)					
Footprint Compatible	FBG676[4]	27 x 27	200, 100 (8)	250, 150 (8)	250, 150 (8)		250, 150 (8)		
	FFG676	27 x 27		250, 150 (8)	250, 150 (8)		250, 150 (8)		
Footprint Compatible	FBG900[4]	31 x 31			350, 150 (16)		350, 150 (16)		
	FFG900	31 x 31			350, 150 (16)		350, 150 (16)		
	FFG901	31 x 31				300, 0 (24)		380, 0 (28)	380, 0 (28)
	FFG1156	35 x 35						400, 0 (32)	400, 0 (32)

Part 2: FPGA Development Board Overview

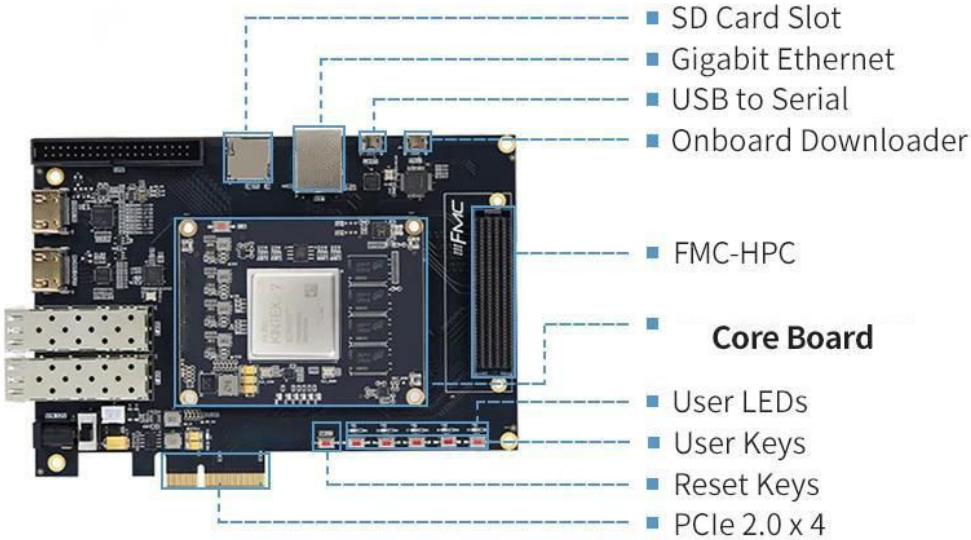
Part 2.1: Board Introduction

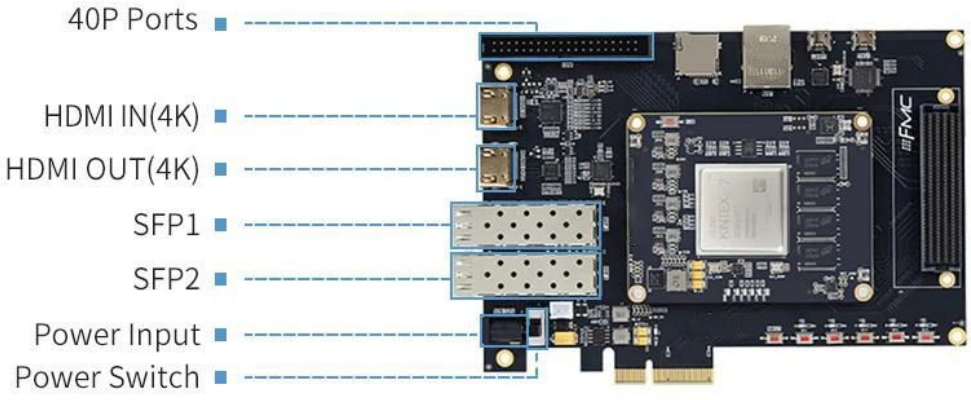
The Kintex7 series FPGA development board has two versions, namely K7-325T and K7-410T. The peripherals of the two versions are fully compatible, and the only difference is the logic capacity of the main chip FPGA.

The Kintex7 series FPGA development board adopts the mode of “core board + Carrier board”. The core board plugs into the carrier board connector through four 120P high-speed connectors. More flexible in use. You can use the core board for both learning and project development.

The FPGA development board integrates rich peripheral resources and provides detailed demos. The board also incorporates the JTAG debugger, a MicroUSB cable, and a 12V power supply to get the board working. More convenient for users.

The from factors of the development board is 156x120mm. A fixed hole is placed at each of the four corners of the core board for mounting support columns or fixing veneers. The aperture is 3.5mm.

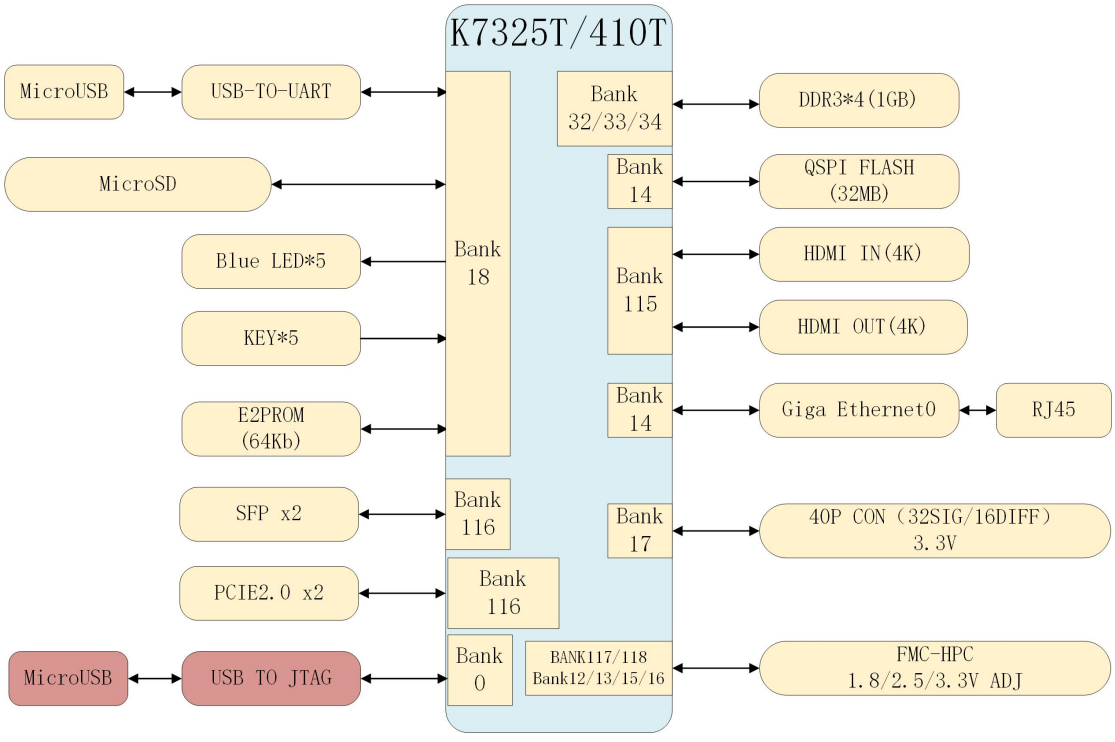




Part 2.2: FPGA Board Resources and Block Diagram

The onboard resources of the FPGA development board are listed in the table and block diagram below, and the functions we have included can be seen from the table below.

CRK7325T-FHB / CRK7410T-FHB FPGA Board Resource		
FPGA	XC7K325T-2FFG900I	XC7K410T-2FFG900I
DDR3	2GB (4 Pics of 512MByte), Data Clock 1600MHZ*64bit	
QSPI FLASH	32MB	
E2PROM	64Kbit	
JTAG	1	
UART	1	
SD Card	1	
Gigabit Ethernet	1	
HDMI	1 HDMI input and output, 1 HDMI output	
LEDs, KEYs	5 LEDs (high-level), 5 Keys (low-level)	
PCIE2.0	x 8	
SFP	2	
40P Expansion Port	1, 32 Single-ended/16 Pairs of Differential	
FMC Expansion Ports	FMC-HPC Type	
Form Factors	SOM Core Board: 83.8mm x 64.8mm; FPGA Board: 165mm x 108mm	
Board to Board Connectors	Four 120P 0.5 high speed connectors, Height is 3mm	
Power Adapter	12V/3A	



Part 3: SOM Core Board Overview

Part 3.1: SOM Introduction

The **CRK7325T/410T** core board is equipped with a Xilinx KINTEX-7 FPGA chip, the model is XC7K325T-2FFG900I/ XC7K410T-FFG900I. The FPGA chip package is FFG900, speed grade is -2, temperature grade is industrial grade. In addition, the core board is also integrated with DDR3/QSPI FLASH/ Gigabit Ethernet and other peripherals

The core board plugs into the carrier board connector through four 120P high-speed connectors, and the core board has four 3.5mm fixing holes placed on the four feet, which can be tightened with the carrier board by screws to ensure stable operation in a strong vibration environment.

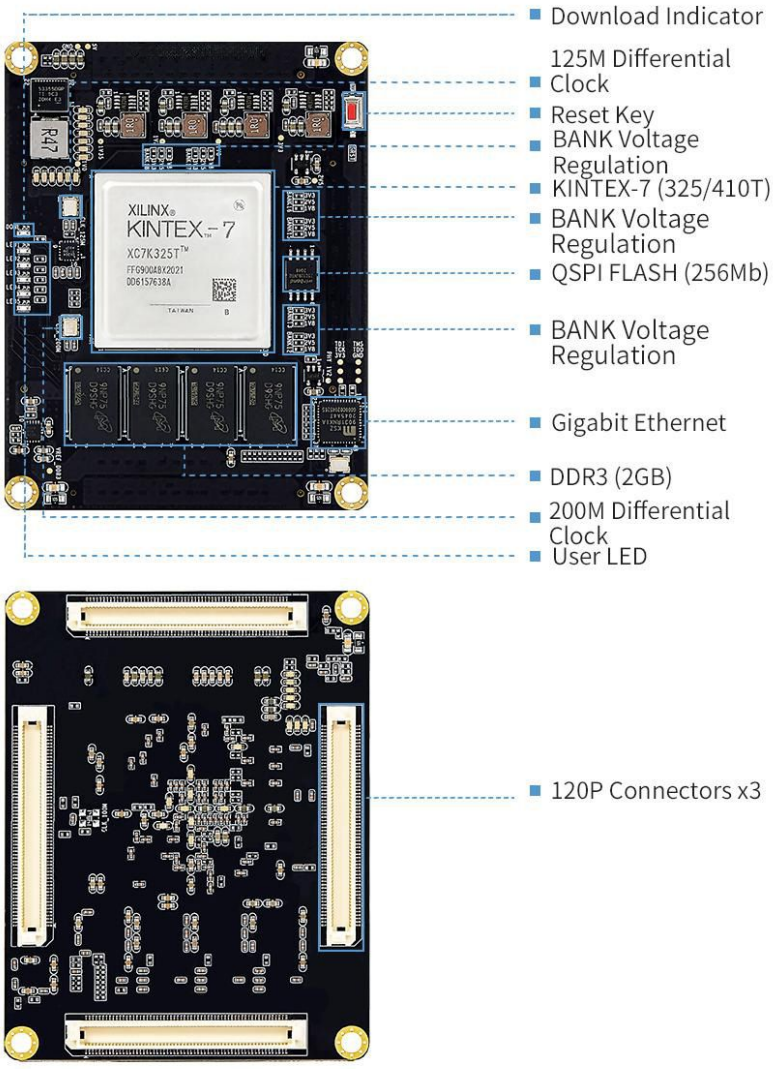
The FPGA development board Demos is written with XC7K325T-FFG900I model. Users can modify the main chip according to the FPGA development board, and other resources are completely the same

Part 3.2: SOM Specification

CRK7325TC/CRK7410C Industrial Grade SOM Specification		
FPGA	XC7K325T-2FFG900I	XC7K410T-2FFG900I
Logic Cells	326080	406720
Flip-Flops	407600	508400
Slices	50950	63550
DSP Slices	840	1540
Block RAM	445	795
DDR3/DD3L	2GB（Data Width 64bit）	
QSPI FLASH	32Mb, to store startup files and user files	
Start Method	JTAG/QSPI FLASH	
Gigabit Ethernet	1	
User LEDs	5 LEDs (High-level on, Low-level off)	
IO Number	288 IOs（ 1.8/2.5/3.3V adjustable, default by 3.3V）	
Number of GTX ports	4 BANK, 16 Paris of TX/RX each	
Working Voltage/Max. Current	5V/3A	
Working Temperature	-40°C~+85°C	
Form Factors	83.8mm x 64.8mm, Immersion Gold Process	
Technology	0.6mm 120P Connectors X 4	
Connectors Height	3mm	

Part 3.3: Product Appearance

The following figure shows the location of each major electronic component on the core board for easy identification.



Part 3.4: SOM Form Factors

The core board size is 83.8 mm x 64.8mm. The core board is connected to the carrier board via four 0.6mm/120P gold-plated high-speed connectors on the bottom.

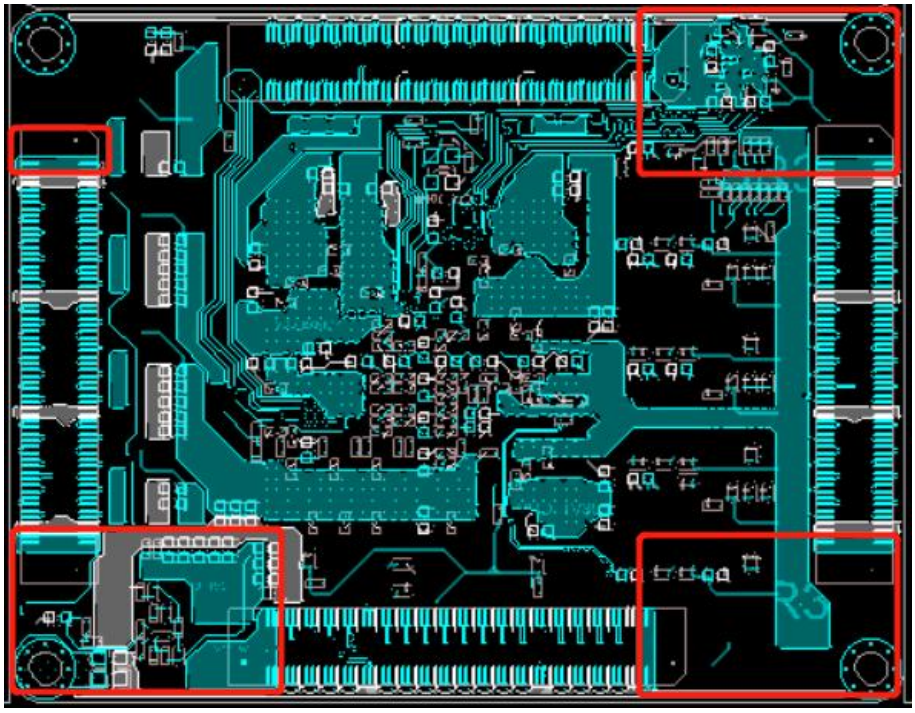


Part 3.5: Power Connection

The power supply voltage range of the FPGA core board is 5V. The Power input pins are reserved at the four corners of the module, and the power pins have been connected inside the module. When designed, it only needs to connect the power pin core board at one corner to work. The power connection needs to be connected with copper and enough holes are made to ensure the power flow ability. All GND signals on the module need to be connected to the base plate, and each GND is connected to the carrier board through two through-holes to ensure through-flow capability. The limit current of the core board is 5V/3A, so the external power supply needs to consider the limit current situation to ensure the stable operation of the core board.

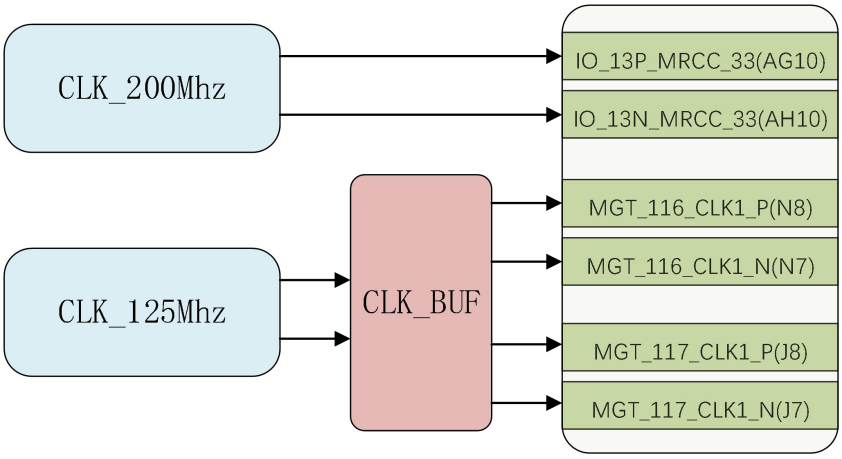
The power supply output voltage of the module power supply needs to be stable, in the module

power supply input plus a level of DCDC power conversion, from high voltage to 5V, DCDC current output capacity can be selected about 5A, such as power chip MP2482 can be referenced. Two **220uF/ 10V** capacitors should be placed in the power input of the core board to ensure the quality of the power supply.



Part 3.6: Clock

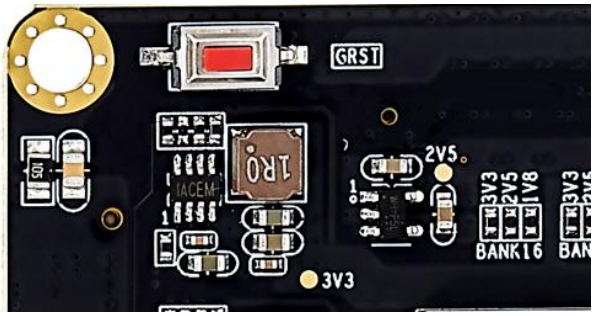
Two active differential crystals are placed on the core board, with a 200M clock providing a differential clock for the logic side and a 125M differential clock for the GTX interface. As shown in the figure below, the 200M differential clock is connected to the 13P/13N pin of BANK33, the corresponding pin position is AG10/AH10, and the 125M clock is converted into two N8/N7 and J8/J7 positions to BANK116/117 respectively



Part 3.7: Global Reset

The core board reserves a reset key for debugging use, this reset key uses RC circuitry, the reset is not sufficient, only used for debugging, the key is connected with the FPGA BANK14, the corresponding pin is "**IO_12P_MRCC_14 (T26)**". Actual products require a reset circuit, and a dedicated reset chip can be used on the carrier board, such as the **MAX811**, or other chips with a longer reset time.





Part 3.8: Boot Mode Selection

The boot mode has been set on the core board, and the system defaults to the "**Master SPI**" boot mode.

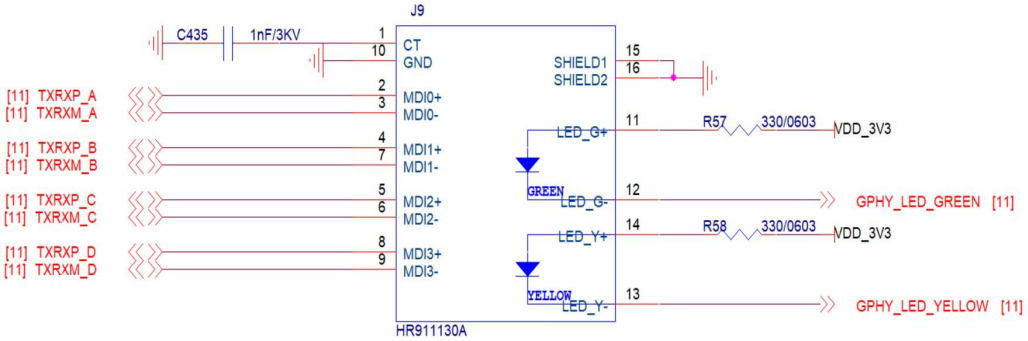
BOOT MODE	M2	M1	M0
JTAG	1	0	1
M SPI	0	0	1

Part 3.9: Gigabit Ethernet Chip

A gigabit Ethernet chip KSZ9031 is placed on the core board, and the Ethernet chip and ZYNQ chip are connected through the RGMII interface. The corresponding pins are shown in the following table. For Ethernet external connection, only an RJ45 with transformer is required, and the chip address is PHY_AD[2:0]=001. The connection schematic diagram can refer to the following figure (the product circuit needs to add an ESD protection circuit).

Note: The product circuit needs to add electrostatic protection on the network port signal line and LED, and the 0.1uF capacitor should be 2KV or 3KV withstanding voltage.

RMGII Signal	Pin Name	Pin Position
TX_CLK	IO_13N_MRCC_14	U28
TXD0	IO_14P_MRCC_14	T25
TXD1	IO_14N_MRCC_14	U25
TXD2	IO_15P_14	U29
TXD3	IO_15N_14	U30
TX_EN	IO_16P_14	V26
RX_CLK	IO_13P_MRCC_14	U27
RXD0	IO_16N_14	V27
RXD1	IO_17P_14	V29
RXD2	IO_17N_14	V30
RXD3	IO_18P_14	V25
RX_CTL	IO_18N_14	W26
PHY_nRST (Power on Reset by Default)	IO_20P_14	W23
MDC	IO_19P_14	V19
MDIO	IO_19N_14	V20



Part 3.10: QSPI FLASH

The FPGA development board has a 32MB QSPI FLASH onboard, the model is MX25L25645GM2I-08G, which can be used to store startup files and user files.



QSPI FLASH PIN	PIN Name	PIN Position
DATA0	IO_1P_14	P24

DATA1	IO_1N_14	R25
DATA2	IO_2P_14	R20
DATA3	IO_2N_14	R21
QSPI_CS	IO_6P_14	R23
QSPI_CLK	CCLK_0	B10

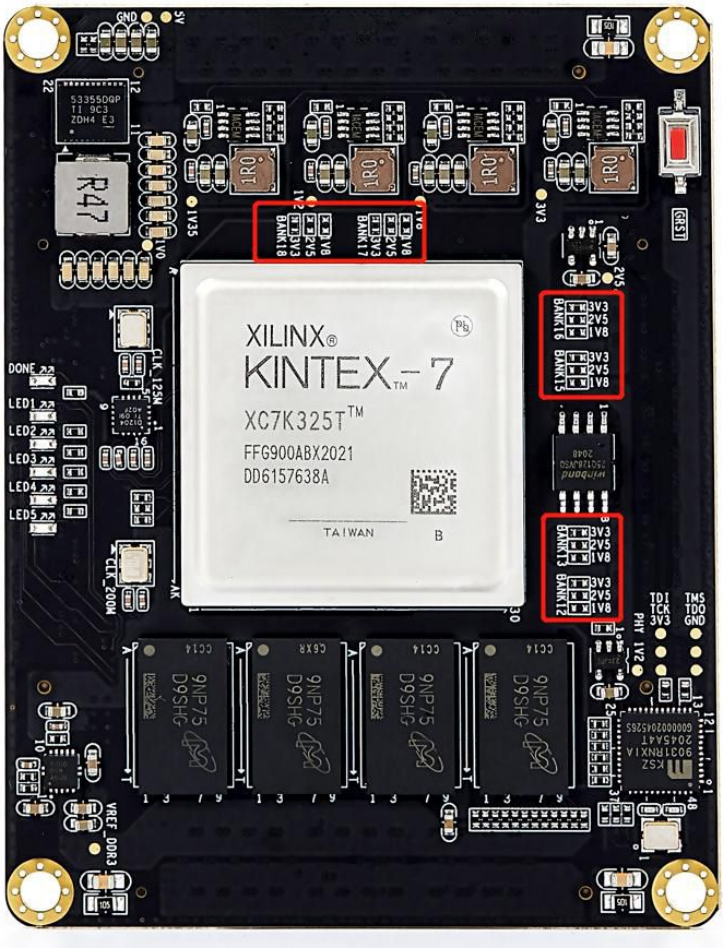
Part 3.11: On-board LED

In order to facilitate debugging, five LEDs are placed on the core board. The pin positions of the LEDs are as shown in the table below. When the pin outputs a high level, the LED lights up, and when the pin outputs a high level, the LED turns off.

LED Pin	Pin Name	Pin Position
LED1	IO_23P_14	U24
LED2	IO_23N_14	V24
LED3	IO_24P_14	W21
LED4	IO_24N_14	W22
LED5	IO_25_14	W19

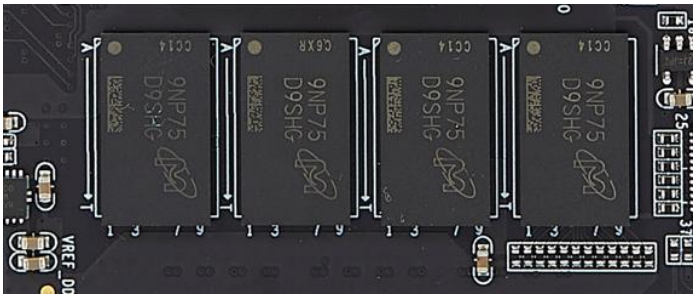
Part 3.12: BANK Interface Level Selection

The external banks on the core board are BANK12/13/14/15/32/33/34. The IOs of these banks can independently support three levels of 1.8V/2.5V/3.3V. The default level of BANK is 3.3V. If you need to change the level, you only need to replace the corresponding position resistor to realize the adjustment. The core board has marked the position of the BANK level adjustment resistor, as shown in the figure below.



Part 3.13: DDR3

The PS side is equipped with four industrial-grade DDR3L chips, with a single capacity of 512MB and a total capacity of 2GB. The model is "**MT41K256M16TW-107IT:P**". DDR3L pin allocation refer to the following table.



DDR3L Pin	Pin Name	Pin Position
DDR3_D0	IO-L4N-32	AG14
DDR3_D1	IO-L5P-32	AH17

DDR3_D2	IO-L1N-32	AK15
DDR3_D3	IO-L4P-32	AF15
DDR3_D4	IO-L1P-32	AK16
DDR3_D5	IO-L6P-32	AE16
DDR3_D6	IO-L2N-32	AH15
DDR3_D7	IO-L5N-32	AJ17
DDR3_DM0	IO-L2P-32	AG15
DDR3_DQS_P0	IO-L3P-32	AH16
DDR3_DQS_N0	IO-L3N-32	AJ16
DDR3_D8	IO-L8N-32	AH19
DDR3_D9	IO-L7N-32	AK19
DDR3_D10	IO-L10P-32	AD19
DDR3_D11	IO-L10N-32	AE19
DDR3_D12	IO-L11P-32	AF18
DDR3_D13	IO-L12N-32	AG17
DDR3_D14	IO-L8P-32	AG19
DDR3_D15	IO-L11N-32	AG18
DDR3_DM1	IO-L12P-32	AF17
DDR3_DQS_P1	IO-L9P-32	AJ18
DDR3_DQS_N1	IO-L9N-32	AK18
DDR3_D16	IO-L17N-32	AC19
DDR3_D17	IO-L18P-32	AB17
DDR3_D18	IO-L18N-32	AC17
DDR3_D19	IO-L16P-32	AA18
DDR3_D20	IO-L14P-32	AD17
DDR3_D21	IO-L16N-32	AB18
DDR3_D22	IO-L13N-32	AE18
DDR3_D23	IO-L17P-32	AB19
DDR3_DM2	IO-L14N-32	AD16
DDR3_DQS_P2	IO-L15P-32	Y19
DDR3_DQS_N2	IO-L15N-32	Y18
DDR3_D24	IO-L20N-32	AB15
DDR3_D25	IO-L23P-32	AA17
DDR3_D26	IO-L24N-32	Y15
DDR3_D27	IO-L19P-32	AE15
DDR3_D28	IO-L20P-32	AA15
DDR3_D29	IO-L22N-32	AD14
DDR3_D30	IO-L24P-32	Y16
DDR3_D31	IO-L22P-32	AC14
DDR3_DM3	IO-L23N-32	AA16
DDR3_DQS_P3	IO-L21P-32	AC16
DDR3_DQS_N3	IO-L21N-32	AC15

DDR3_D32	IO-L6P-34	AC7
DDR3_D33	IO-L1P-34	AD4
DDR3_D34	IO-L4N-34	AC4
DDR3_D35	IO-L5N-34	AE6
DDR3_D36	IO-L4P-34	AC5
DDR3_D37	IO-L5P-34	AD6
DDR3_D38	IO-L2N-34	AC1
DDR3_D39	IO-L1N-34	AD3
DDR3_DM4	IO-L2P-34	AC2
DDR3_DQS_P4	IO-L3P-34	AD2
DDR3_DQS_N4	IO-L3N-34	AD1
DDR3_D40	IO-L7N-34	AF2
DDR3_D41	IO-L7P-34	AF3
DDR3_D42	IO-L11N-34	AF5
DDR3_D43	IO-L8P-34	AE1
DDR3_D44	IO-L11P-34	AE5
DDR3_D45	IO-L10N-34	AE3
DDR3_D46	IO-L12P-34	AF6
DDR3_D47	IO-L10P-34	AE4
DDR3_DM5	IO-L8N-34	AF1
DDR3_DQS_P5	IO-L9P-34	AG4
DDR3_DQS_N5	IO-L9N-34	AG3
DDR3_D48	IO-L16P-34	AH2
DDR3_D49	IO-L13N-34	AJ4
DDR3_D50	IO-L16N-34	AJ2
DDR3_D51	IO-L13P-34	AH4
DDR3_D52	IO-L17N-34	AK1
DDR3_D53	IO-L14P-34	AH6
DDR3_D54	IO-L17P-34	AJ1
DDR3_D55	IO-L18P-34	AJ3
DDR3_DM6	IO-L14N-34	AH5
DDR3_DQS_P6	IO-L15P-34	AG2
DDR3_DQS_N6	IO-L15N-34	AH1
DDR3_D56	IO-L23N-34	AK8
DDR3_D57	IO-L22N-34	AK6
DDR3_D58	IO-L23P-34	AJ8
DDR3_D59	IO-L24N-34	AK4
DDR3_D60	IO-L20P-34	AF7
DDR3_D61	IO-L24P-34	AK5
DDR3_D62	IO-L19P-34	AF8
DDR3_D63	IO-L22P-34	AJ6
DDR3_DM7	IO-L20N-34	AG7

DDR3_DQS_P7	IO-L21P-34	AH7
DDR3_DQS_N7	IO-L21N-34	AJ7
DDR3_A0	IO-L18P-33	AH11
DDR3_A1	IO-L21P-33	AH14
DDR3_A2	IO-L7N-33	AC10
DDR3_A3	IO-L10N-33	AE9
DDR3_A4	IO-L15N-33	AK9
DDR3_A5	IO-L8N-33	AE8
DDR3_A6	IO-L19P-33	AE13
DDR3_A7	IO-L10P-33	AD9
DDR3_A8	IO-L23P-33	AF12
DDR3_A9	IO-L9P-33	AC12
DDR3_A10	IO-L18N-33	AJ11
DDR3_A11	IO-L20N-33	AK13
DDR3_A12	IO-L14P-33	AE10
DDR3_A13	IO-L7P-33	AB10
DDR3_A14	IO-L22N-33	AJ12
DDR3_BA0	IO-L22P-33	AJ13
DDR3_BA1	IO-L21N-33	AJ14
DDR3_BA2	IO-L9N-33	AC11
DDR3_CS	IO-L16P-33	AG9
DDR3_RAS	IO-L14N-33	AF10
DDR3_CAS	IO-L17P-33	AK11
DDR3_WE	IO-L16N-33	AH9
DDR3_ODT	IO-L20P-33	AK14
DDR3_RESET	IO-L8P-33	AD8
DDR3_CLK_P	IO-L12P-33	AD12
DDR3_CLK_N	IO-L12N-33	AD11
DDR3_CKE	IO-L17N-33	AK10

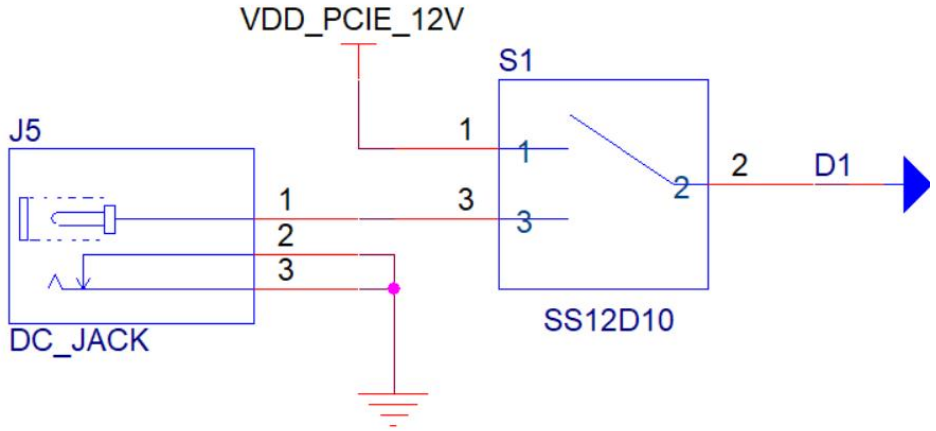
Part 4: Carrier Board Overview

Part 4.1: Power Supply and BANK Voltage Regulation

The FPGA development board provides two power supply modes: PCIE interface and 12V/3A power adapter. The two power supply options can be selected by DIP switch S1 on the FPGA development board. If switch S1 is moved to a position close to the DC005 plug, the external adapter is used for power supply. If switch S1 is moved to the other side, the PCIE interface is powered.

After the 12V power supply enters the FPGA development board, it is converted into 5V/3.3V power supply through the secondary power supply, which is used by the core board and the internal and external peripherals of the board. Detailed circuit can refer to the schematic diagram of the FPGA development board.

In addition, the level of each BANK on the core board can be adjusted by 1.8/2.5/3.3V independently. The default level is 3.3V. If you need to adjust the voltage, you can adjust the resistance corresponding to the BANK. For details, refer to part 2.8 of the Core Board user manual.

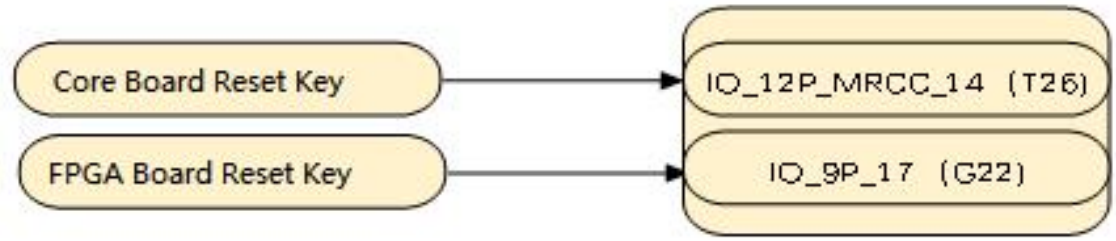


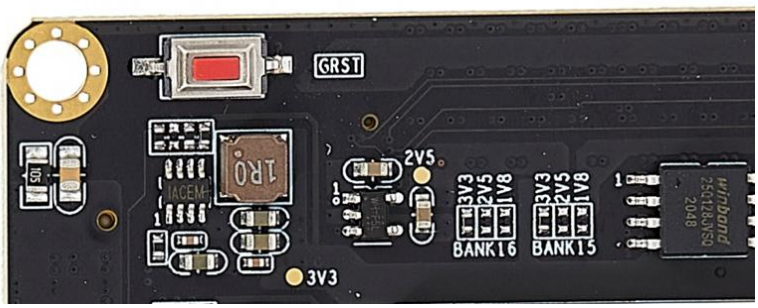
Part 4.2: System Reset

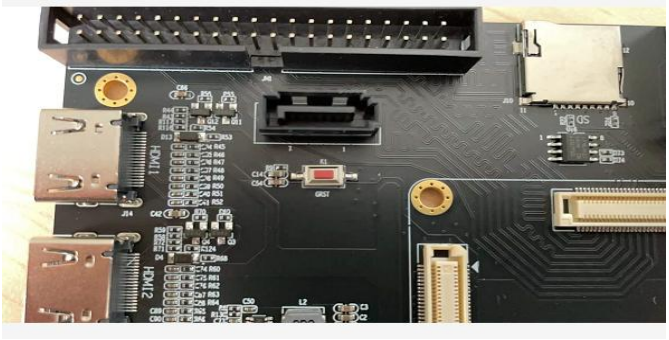
A reset circuit is reserved on the FPGA Carrier board and the SOM core board respectively, the user can choose which one to use according to the actual use.

The reset pin on the core board is connected to BANK14 of the FPGA and the corresponding pin is IO_12P_MRCC_14(T26). The reset pin on the FPGA board is connected to BANK17 of the FPGA and the corresponding pin is IO_9P_17(G22).

If the actual product needs to add reset circuit, you can use a special reset chip on the carrier board, such as MAX811, the user can choose according to the needs.







Part 4.3: Boot Mode Selection

The boot mode has been set on the core board, and the system defaults to the "**Master SPI**" boot mode.

BOOT MODE	M2	M1	M0
JTAG	1	0	1
M SPI	0	0	1

Part 4.4: DDR3

The core board contains four industrial-grade DDR3L chips with a single capacity of 512MB and a total capacity of 2GB. The model is "**MT41K256M16TW-107IT:P**", DDR3L pin allocation see the following table.



DDR3L Pin	Pin Name	Pin Position
DDR3_D0	IO-L4N-32	AG14
DDR3_D1	IO-L5P-32	AH17
DDR3_D2	IO-L1N-32	AK15
DDR3_D3	IO-L4P-32	AF15
DDR3_D4	IO-L1P-32	AK16
DDR3_D5	IO-L6P-32	AE16
DDR3_D6	IO-L2N-32	AH15
DDR3_D7	IO-L5N-32	AJ17
DDR3_DM0	IO-L2P-32	AG15
DDR3_DQS_P0	IO-L3P-32	AH16
DDR3_DQS_N0	IO-L3N-32	AJ16
DDR3_D8	IO-L8N-32	AH19
DDR3_D9	IO-L7N-32	AK19
DDR3_D10	IO-L10P-32	AD19
DDR3_D11	IO-L10N-32	AE19
DDR3_D12	IO-L11P-32	AF18
DDR3_D13	IO-L12N-32	AG17
DDR3_D14	IO-L8P-32	AG19
DDR3_D15	IO-L11N-32	AG18
DDR3_DM1	IO-L12P-32	AF17
DDR3_DQS_P1	IO-L9P-32	AJ18
DDR3_DQS_N1	IO-L9N-32	AK18
DDR3_D16	IO-L17N-32	AC19
DDR3_D17	IO-L18P-32	AB17
DDR3_D18	IO-L18N-32	AC17
DDR3_D19	IO-L16P-32	AA18
DDR3_D20	IO-L14P-32	AD17
DDR3_D21	IO-L16N-32	AB18
DDR3_D22	IO-L13N-32	AE18
DDR3_D23	IO-L17P-32	AB19
DDR3_DM2	IO-L14N-32	AD16
DDR3_DQS_P2	IO-L15P-32	Y19

DDR3_DQS_N2	IO-L15N-32	Y18
DDR3_D24	IO-L20N-32	AB15
DDR3_D25	IO-L23P-32	AA17
DDR3_D26	IO-L24N-32	Y15
DDR3_D27	IO-L19P-32	AE15
DDR3_D28	IO-L20P-32	AA15
DDR3_D29	IO-L22N-32	AD14
DDR3_D30	IO-L24P-32	Y16
DDR3_D31	IO-L22P-32	AC14
DDR3_DM3	IO-L23N-32	AA16
DDR3_DQS_P3	IO-L21P-32	AC16
DDR3_DQS_N3	IO-L21N-32	AC15
DDR3_D32	IO-L6P-34	AC7
DDR3_D33	IO-L1P-34	AD4
DDR3_D34	IO-L4N-34	AC4
DDR3_D35	IO-L5N-34	AE6
DDR3_D36	IO-L4P-34	AC5
DDR3_D37	IO-L5P-34	AD6
DDR3_D38	IO-L2N-34	AC1
DDR3_D39	IO-L1N-34	AD3
DDR3_DM4	IO-L2P-34	AC2
DDR3_DQS_P4	IO-L3P-34	AD2
DDR3_DQS_N4	IO-L3N-34	AD1
DDR3_D40	IO-L7N-34	AF2
DDR3_D41	IO-L7P-34	AF3
DDR3_D42	IO-L11N-34	AF5
DDR3_D43	IO-L8P-34	AE1
DDR3_D44	IO-L11P-34	AE5
DDR3_D45	IO-L10N-34	AE3
DDR3_D46	IO-L12P-34	AF6
DDR3_D47	IO-L10P-34	AE4
DDR3_DM5	IO-L8N-34	AF1
DDR3_DQS_P5	IO-L9P-34	AG4
DDR3_DQS_N5	IO-L9N-34	AG3
DDR3_D48	IO-L16P-34	AH2
DDR3_D49	IO-L13N-34	AJ4
DDR3_D50	IO-L16N-34	AJ2
DDR3_D51	IO-L13P-34	AH4
DDR3_D52	IO-L17N-34	AK1
DDR3_D53	IO-L14P-34	AH6
DDR3_D54	IO-L17P-34	AJ1
DDR3_D55	IO-L18P-34	AJ3

DDR3_DM6	IO-L14N-34	AH5
DDR3_DQS_P6	IO-L15P-34	AG2
DDR3_DQS_N6	IO-L15N-34	AH1
DDR3_D56	IO-L23N-34	AK8
DDR3_D57	IO-L22N-34	AK6
DDR3_D58	IO-L23P-34	AJ8
DDR3_D59	IO-L24N-34	AK4
DDR3_D60	IO-L20P-34	AF7
DDR3_D61	IO-L24P-34	AK5
DDR3_D62	IO-L19P-34	AF8
DDR3_D63	IO-L22P-34	AJ6
DDR3_DM7	IO-L20N-34	AG7
DDR3_DQS_P7	IO-L21P-34	AH7
DDR3_DQS_N7	IO-L21N-34	AJ7
DDR3_A0	IO-L18P-33	AH11
DDR3_A1	IO-L21P-33	AH14
DDR3_A2	IO-L7N-33	AC10
DDR3_A3	IO-L10N-33	AE9
DDR3_A4	IO-L15N-33	AK9
DDR3_A5	IO-L8N-33	AE8
DDR3_A6	IO-L19P-33	AE13
DDR3_A7	IO-L10P-33	AD9
DDR3_A8	IO-L23P-33	AF12
DDR3_A9	IO-L9P-33	AC12
DDR3_A10	IO-L18N-33	AJ11
DDR3_A11	IO-L20N-33	AK13
DDR3_A12	IO-L14P-33	AE10
DDR3_A13	IO-L7P-33	AB10
DDR3_A14	IO-L22N-33	AJ12
DDR3_BA0	IO-L22P-33	AJ13
DDR3_BA1	IO-L21N-33	AJ14
DDR3_BA2	IO-L9N-33	AC11
DDR3_CS	IO-L16P-33	AG9
DDR3_RAS	IO-L14N-33	AF10
DDR3_CAS	IO-L17P-33	AK11
DDR3_WE	IO-L16N-33	AH9
DDR3_ODT	IO-L20P-33	AK14
DDR3_RESET	IO-L8P-33	AD8
DDR3_CLK_P	IO-L12P-33	AD12
DDR3_CLK_N	IO-L12N-33	AD11
DDR3_CKE	IO-L17N-33	AK10

Part 4.5: QSPI FLASH

The FPGA development board has a 32MB QSPI FLASH onboard, the model is MX25L25645GM2I-08G, which can be used to store startup files and user files.



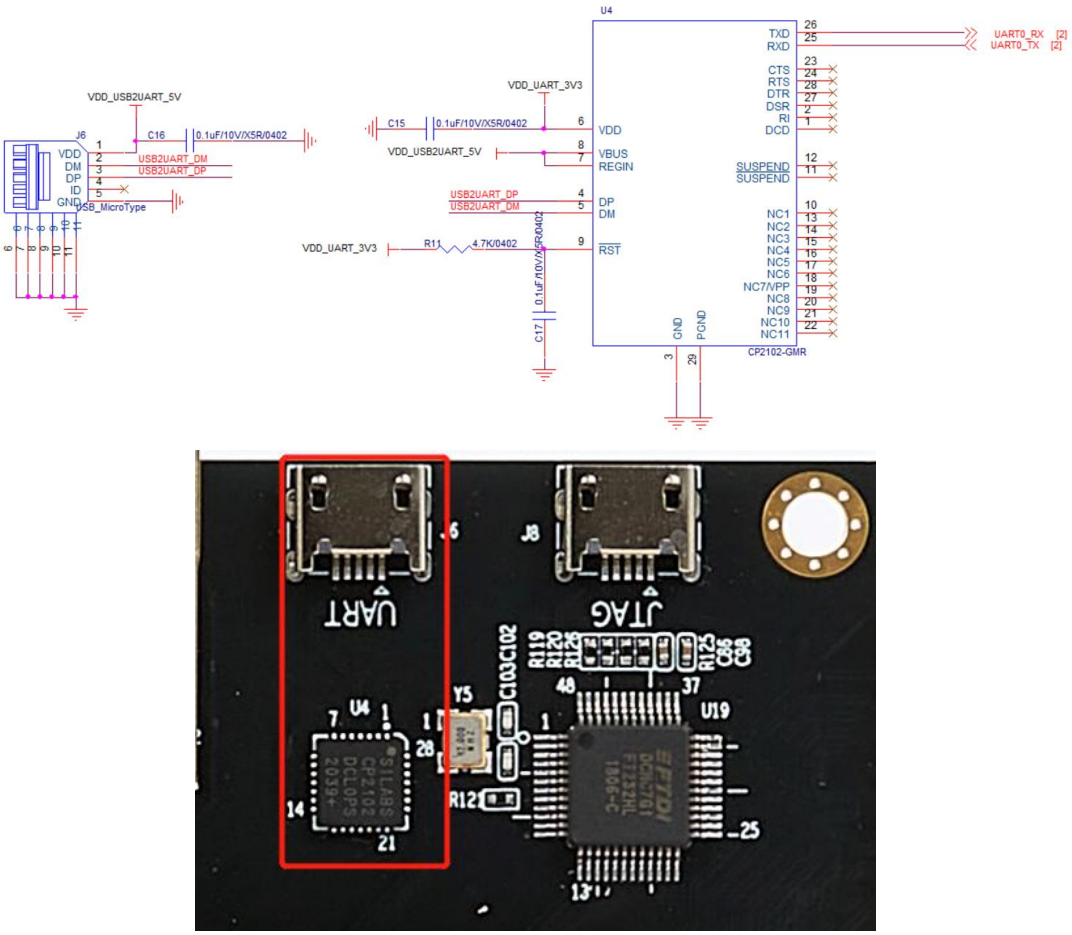
QSPI FLASH PIN	PIN Name	PIN Position
DATA0	IO_1P_14	P24
DATA1	IO_1N_14	R25
DATA2	IO_2P_14	R20
DATA3	IO_2N_14	R21
QSPI_CS	IO_6P_14	R23
QSPI_CLK	CCLK_0	B10

Part 4.6: USB to UART

The FPGA development board uses "**Silicon Labs CP2102GM**" chip to realize USB to UART, and the USB interface adopts "**Micro USB**". Users only need to use a Micro USB cable to connect to the PC for serial communication.

The "**TX/RX**" signal of the UART is connected with the "**BANK15**" of the "**FPGA**", and the interface level is 3.3V. The following is the signal correspondence table and schematic diagram, the TX/RX direction is defined for the MPSOC side.

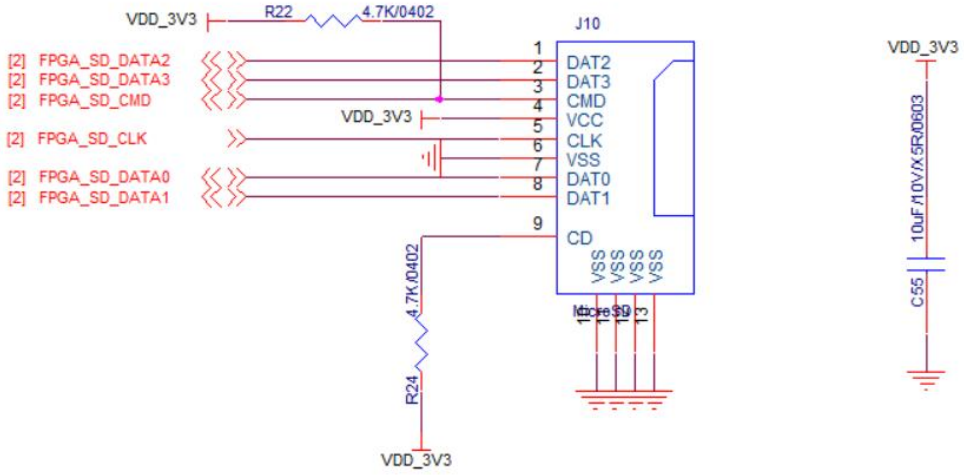
UART0 Pin	FPGA Pin Name	Pin Position
UART0_TX	IO-5P-18	K14
UART0_RX	IO-5N-18	J14

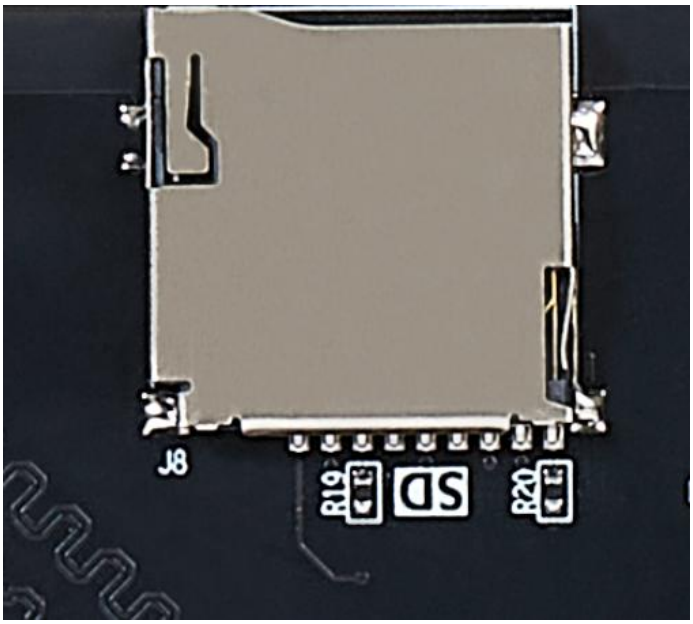


Part 4.7: SD Card

A TF card holder is placed on the FPGA development board, which is convenient for users to store files. The circuit interface level is "**3.3V**", the SD card signal is connected to the "BANK18" of the FPGA. The following is the signal correspondence table and schematic. The TX/RX direction is defined for the FPGA end

SD Card Pin	FPGA Pin Name	Pin Position
SD-CLK	IO-24N-18	A15
SD-CMD	IO-9N-18	H16
SD-DATA0	IO-7P-18	H15
SD-DATA1	IO-22P-18	B13
SD-DATA2	IO-7N-18	G15
SD-DATA3	IO-22N-18	A13



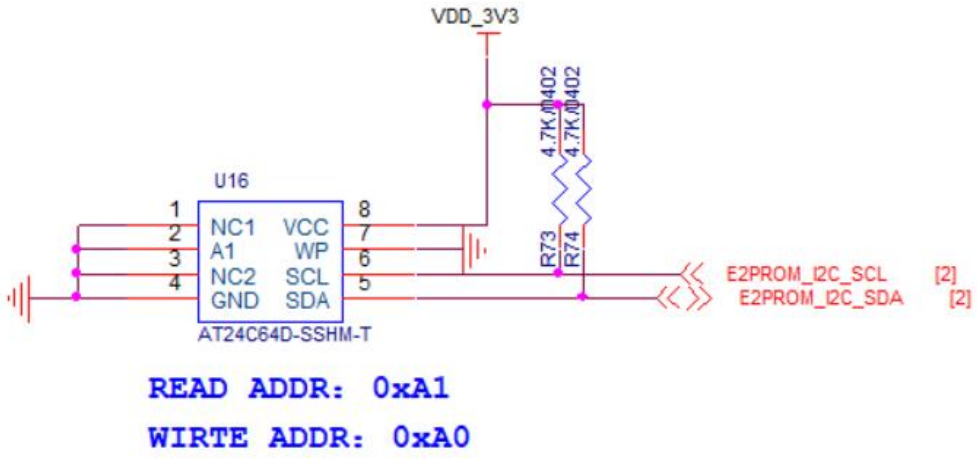


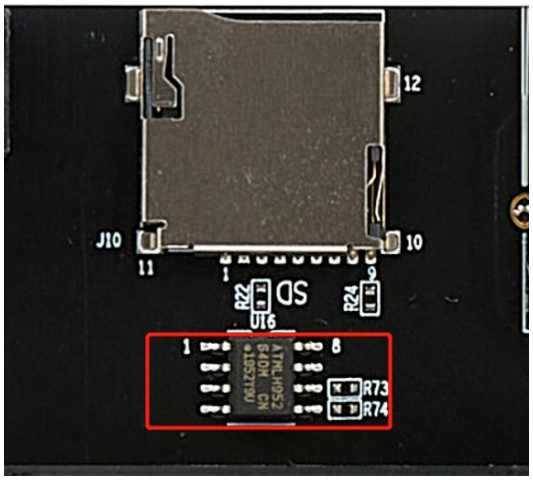
Part 4.8: E2PROM

A 64Kbit EEPROM chip, AT24C64D-SSHM-T, is placed on the FPGA Carrier board, which is connected to BANK18 of FPGA through IIC bus. The read address of EEPROM is 0xA1 and the write address is 0xA0.

The following is the pin assignment and schematic diagram of EEPROM.

EEPROM Pin	FPGA Pin Name	Pin Position
E2PROM_I2C_SCL	IO-1P-18	L16
E2PROM_I2C_SDA	IO-1N-18	K16





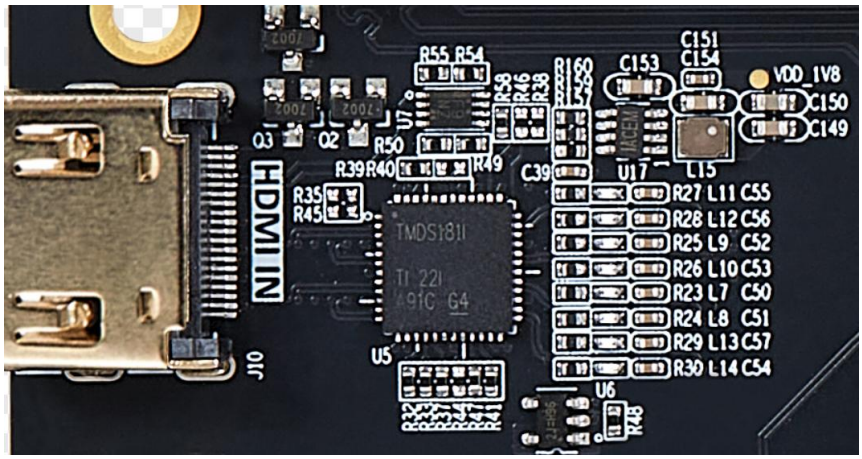
Part 4.9: HDMI Input Interface (4K 60FPS)

One HDMI input interface is designed on the FPGA Carrier Board, which can achieve 4K/60FPS image input, multiple resolutions and frame rates are adjustable.

The following is the HDMI pin allocation, the schematic diagram can be viewed in the folder.

HDMI Input	FPGA Pin Name	Pin Position
GTX_HDMI_IN_P0	MGT_RX_P0_115	AA4
GTX_HDMI_IN_N0	MGT_RX_N0_115	AA3
GTX_HDMI_IN_P1	MGT_RX_P1_115	Y6
GTX_HDMI_IN_N1	MGT_RX_N1_115	Y5
GTX_HDMI_IN_P2	MGT_RX_P2_115	W4
GTX_HDMI_IN_N2	MGT_RX_N2_115	W3
GTX_HDMI_IN_CLK_P	MGT_CLK0_P_115	R8
GTX_HDMI_IN_CLK_N	MGT_CLK0_N_115	R7
F_HDMI_IN_HPD	IO_L1N_17	J18
F_HDMI_SCL_CTL	IO_L17P_17	C17
F_HDMI_SDA_CTL	IO_L17N_17	B17

HDMI_IN_PWR_DET	IO_L18P_17	G17
F_HDMI_IN_I2C_SCL	IO_L18N_17	F17
F_HDMI_IN_I2C_SDA	IO_L1P_17	K18

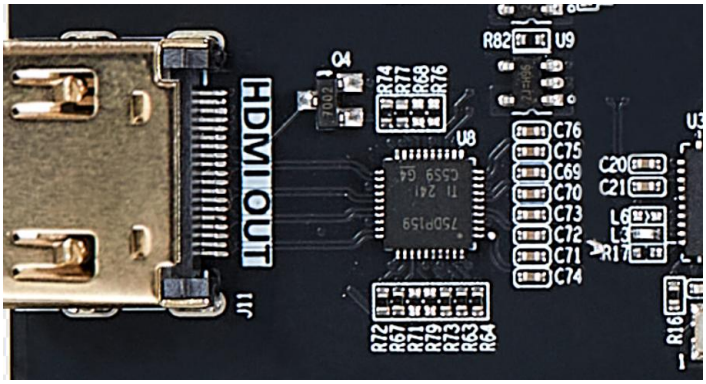


Part 4.10: HDMI Output Interface (4K 60FPS)

One HDMI output interface is designed on the FPGA Carrier Board, which can achieve 4K/60FPS image output, multiple resolutions and frame rates are adjustable.

The following is the HDMI pin allocation, the schematic diagram can be viewed in the folder.

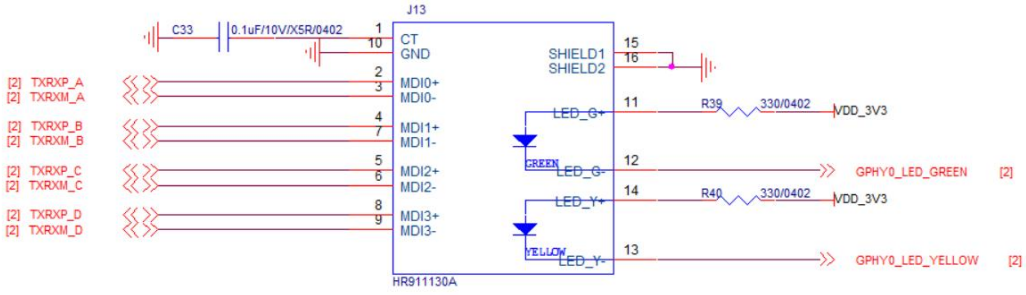
HDMI Output	FPGA Pin Name	Pin Position
GTX_HDMI_OUT_P0	MGT_TX_P0_115	Y2
GTX_HDMI_OUT_N0	MGT_TX_N0_115	Y1
GTX_HDMI_OUT_P1	MGT_TX_P1_115	V2
GTX_HDMI_OUT_N1	MGT_TX_N1_115	V1
GTX_HDMI_OUT_P2	MGT_TX_P2_115	U4
GTX_HDMI_OUT_N2	MGT_TX_N2_115	U3
GTX_HDMI_CLK_P	MGT_CLK1_P_115	U8
GTX_HDMI_CLK_N	MGT_CLK1_N_115	U7
GTX_HDMI_OUT_CLK_P	IO_L13P_MRCC_16	D27
GTX_HDMI_OUT_CLK_N	IO_L13N_MRCC_16	C27
F_HDMI_OUT_HPD	IO_L20P_17	A16
F_HDMI_OUT_SCL_SRC	IO_L16P_17	G18
F_HDMI_OUT_SDA_SRC	IO_L16N_17	F18
F_HDMI_SCL_CTL	IO_L17P_17	C17
F_HDMI_SDA_CTL	IO_L17N_17	B17
F_HDMI_OUT_OE	IO_L20N_17	A17
F_HDMI_OUT_CEC	IO_L15P_17	D16

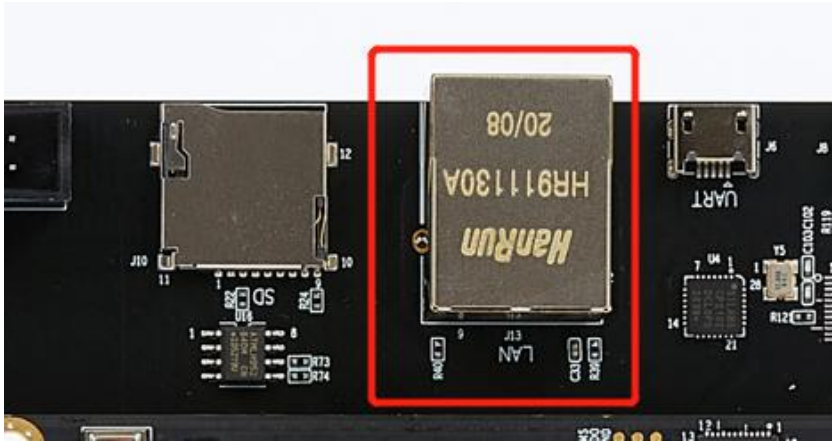


Part 4.11: Gigabit Ethernet

One Gigabit Ethernet chips are placed on the FPGA development board and has been integrated into the core board. The Ethernet chip is interconnected with the FPGA through the RGMII interface. The corresponding pins are shown in the table below. For Ethernet external connection, only one RJ45 with transformer is needed, and the chip address is **PHY_AD[2:0]=001**. For the connection principle, refer to the following figure (ESD protection circuit is required for the product circuit).

RMGII Signal	Pin Name	Pin Position
TX_CLK	IO_13N_MRCC_14	U28
TXD0	IO_14P_MRCC_14	T25
TXD1	IO_14N_MRCC_14	U25
TXD2	IO_15P_14	U29
TXD3	IO_15N_14	U30
TX_EN	IO_16P_14	V26
RX_CLK	IO_13P_MRCC_14	U27
RXD0	IO_16N_14	V27
RXD1	IO_17P_14	V29
RXD2	IO_17N_14	V30
RXD3	IO_18P_14	V25
RX_CTL	IO_18N_14	W26
PHY_nRST	IO_20P_14	W23
MDC	IO_19P_14	V19
MDIO	IO_19N_14	V20





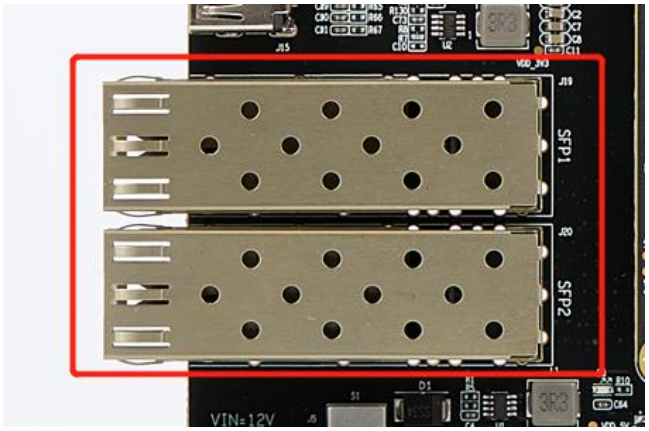
Part 4.12: SFP

Two SFP interfaces are designed on the FPGA development board, and the interface signals are connected with BANK18/BANK118 of FPGA. For details, please refer to the schematic diagram.

The following is the pin distribution of SFP. The schematic diagram can be viewed in the folder.

SFP2 Pin	FPGA Pin Name	Pin Position
SFP-TX-P1	MGT-TX-P0-116	P2
SFP-TX-N1	MGT-TX-N0-116	P1
SFP-RX-P1	MGT-RX-P0-116	T6
SFP-RX-N1	MGT-RX-N0-116	T5
SFP1-TX-DISABLE	IO-16P-18	F11

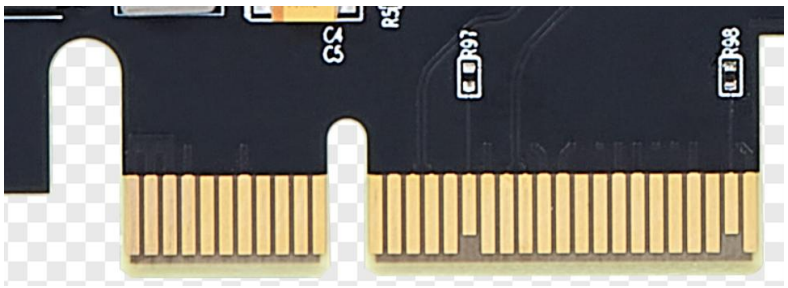
SFP2 Pin	FPGA Pin Name	Pin Position
SFP-TX-P2	MGT-TX-P1-116	N4
SFP-TX-N2	MGT-TX-N1-116	N3
SFP-RX-P2	MGT-RX-P1-116	R4
SFP-RX-N2	MGT-RX-N1-116	R3
SFP2-TX-DISABLE	IO-16N-18	E11



Part 4.13: PCIE Interface

The PCIE2.0 x 2 interface is designed on the FPGA development board, and the interface signal is connected with BANK18/BANK116 of FPGA. The detailed schematic diagram can be referred to.

Signal	FPGA Pin Name	Pin Position
PERST_N	IO_13N_MRCC_18	D13
REF_CLK_P	MGT_116_CLK_P0	L8
REF_CLK_N	MGT_116_CLK_N0	L7
PER0_P	MGT_116_TX_P3	L4
PER0_N	MGT_116_TX_N3	L3
PER1_P	MGT_116_TX_P2	M2
PER1_N	MGT_116_TX_N2	M1
PET0_P	MGT_116_RX_P3	M6
PET0_N	MGT_116_RX_N3	M5
PET1_P	MGT_116_RX_P2	P6
PET1_N	MGT_116_RX_N2	P5



Part 4.14: 40P Expansion Ports

The FPGA development board is equipped with a simple 40P 2.54mm pitch horn holder for extended signal connection. The signal is connected to the BANK16 of the FPGA, the level can be adjusted to 1.8/2.5/3.3V, the default is 3.3V, if you need to modify the level, you need to find the corresponding BANK adjustment resistor on the core board, and the modification can be achieved. The following table indicates the location of the chip where the signal is located, and the detailed connection relationship reference schematic part.

JM1 Signal	ZYNQ Pin Name	Pin Position
5	IO_L9P_16	G22
7	IO_L9N_16	F22
9	IO_L7P_16	H21
11	IO_L7N_16	H22
13	IO_L12P_16	F20
15	IO_L12N_16	E20
17	IO_L2P_16	H20
19	IO_L2N_16	G20

21	IO_L10P_16	D22
23	IO_L10N_16	C22
25	IO_L4P_16	J19
27	IO_L4N_16	H19
29	IO_L14P_16	E19
31	IO_L14N_16	D19
37	IO_L6P_16	K19
39	IO_L6N_16	K20
6	IO_L23P_16	B22
8	IO_L23N_16	A22
10	IO_L8P_16	D21
12	IO_L8N_16	C21
14	IO_L11P_SRCC_16	F21
16	IO_L11N_SRCC_16	E21
18	IO_L19P_16	C20
20	IO_L19N_16	B20
22	IO_L24P_16	C19
24	IO_L24N_16	B19
26	IO_L13P_MRCC_16	D17
28	IO_L13N_MRCC_16	D18
30	IO_L22P_16	B18
32	IO_L22N_16	A18
38	IO_L21P_16	A20
40	IO_L21N_16	A21



Part 4.15: FMC Expansion Ports

One way FMC-HPC connector is designed on the development board, and the following table lists the signal correspondences. Refer to the schematic section for detailed connections.

FMC-HPC Pin	FPGA Pin Name	Pin Position
LA00_P_CC	IO_L11P_SRCC_12	AE23
LA00_N_CC	IO_ L11N_SRCC_12	AF23
LA01_P_CC	IO_L14P_SRCC_12	AG24
LA01_N_CC	IO_ L14N_SRCC_12	AH24
LA02_P	IO_L6P_12	AA20
LA02_N	IO_L6N_12	AB20
LA03_P	IO_L2P_12	Y21
LA03_N	IO_L2N_12	AA21

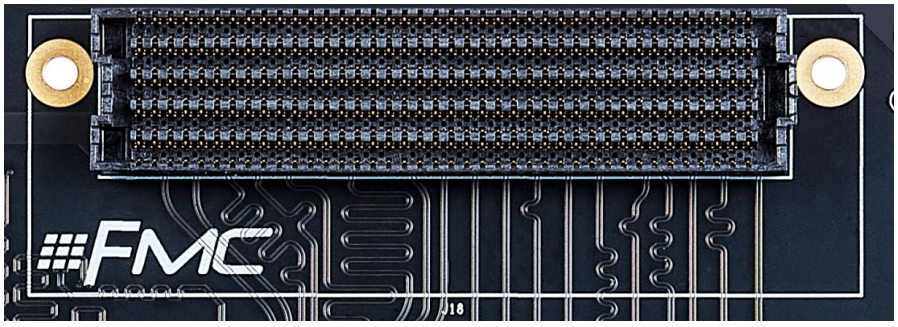
LA04_P	IO_L1P_12	Y23
LA04_N	IO_L1N_12	Y24
LA05_P	IO_L19P_12	AF20
LA05_N	IO_L19N_12	AF21
LA06_P	IO_L5P_12	AC20
LA06_N	IO_L5N_12	AC21
LA07_P	IO_L4P_12	AA22
LA07_N	IO_L4N_12	AA23
LA08_P	IO_L10P_12	AD21
LA08_N	IO_L10N_12	AE21
LA09_P	IO_L22P_12	AG20
LA09_N	IO_L22N_12	AH20
LA10_P	IO_L3P_12	AB22
LA10_N	IO_L3N_12	AB23
LA11_P	IO_L7P_12	AB24
LA11_N	IO_L7N_12	AC25
LA12_P	IO_L8P_12	AC22
LA12_N	IO_L8N_12	AD22
LA13_P	IO_L23P_12	AH21
LA13_N	IO_L23N_12	AJ21
LA14_P	IO_L24P_12	AK20
LA14_N	IO_L24N_12	AK21
LA15_P	IO_L15P_12	AJ24
LA15_N	IO_L15N_12	AK25
LA16_P	IO_L17P_12	AK23
LA16_N	IO_L17N_12	AK24
LA17_P_CC	IO_L12P_MRCC_12	AD23
LA17_N_CC	IO_L12N_MRCC_12	AE24
LA18_P_CC	IO_L13P_MRCC_12	AF22
LA18_N_CC	IO_L13N_MRCC_12	AG23
LA19_P	IO_L9P_12	AC24
LA19_N	IO_L9N_12	AD24
LA20_P	IO_L16P_12	AE25
LA20_N	IO_L16N_12	AF25
LA21_P	IO_L18P_12	AG25
LA21_N	IO_L18N_12	AH25
LA22_P	IO_L21P_12	AJ22
LA22_N	IO_L21N_12	AJ23
LA23_P	IO_L20P_12	AG22
LA23_N	IO_L20N_12	AH22
LA24_P	IO_L4P_16	E24
LA24_N	IO_L4N_16	D24
LA25_P	IO_L6P_16	G23
LA25_N	IO_L6N_16	G24
LA26_P	IO_L23P_16	H26
LA26_N	IO_L23N_16	H27
LA27_P	IO_L5P_16	F26

LA27_N	IO_L5N_16	E26
LA28_P	IO_L19P_16	H24
LA28_N	IO_L19N_16	H25
LA29_P	IO_L3P_16	F25
LA29_N	IO_L3N_16	E25
LA30_P	IO_L21P_16	G27
LA30_N	IO_L21N_16	F27
LA31_P	IO_L9P_16	B28
LA31_N	IO_L9N_16	A28
LA32_P	IO_L24P_16	H30
LA32_N	IO_L24N_16	G30
LA33_P	IO_L22P_16	G29
LA33_N	IO_L22N_16	F30
FMC_IIC_SCL	IO_L23P_18	C15
FMC_IIC_SDA	IO_L23N_18	B15
DP0_M2C_P	MGT_RX_P0_117	K6
DP0_M2C_N	MGT_RX_N0_117	K5
DP1_M2C_P	MGT_RX_P1_117	H6
DP1_M2C_N	MGT_RX_N1_117	H5
DP2_M2C_P	MGT_RX_P2_117	G4
DP2_M2C_N	MGT_RX_N2_117	G3
DP3_M2C_P	MGT_RX_P3_117	F6
DP3_M2C_N	MGT_RX_N3_117	F5
DP4_M2C_P	MGT_RX_P0_118	E4
DP4_M2C_N	MGT_RX_N0_118	E3
DP5_M2C_P	MGT_RX_P1_118	D6
DP5_M2C_N	MGT_RX_N1_118	D5
DP6_M2C_P	MGT_RX_P2_118	B6
DP6_M2C_N	MGT_RX_N2_118	B5
DP7_M2C_P	MGT_RX_P3_118	A8
DP7_M2C_N	MGT_RX_N3_118	A7
GBTCLK0_M2C_P	MGT_CLK0_P_117	G8
GBTCLK0_M2C_N	MGT_CLK0_N_117	G7
GBTCLK1_M2C_P	MGT_CLK0_P_118	C8
GBTCLK1_M2C_N	MGT_CLK0_N_118	C7
DP0_C2M_P	MGT_TX_P0_117	K2
DP0_C2M_N	MGT_TX_N0_117	K1
DP1_C2M_P	MGT_TX_P1_117	J4
DP1_C2M_N	MGT_TX_N1_117	J3
DP2_C2M_P	MGT_TX_P2_117	H2
DP2_C2M_N	MGT_TX_N2_117	H1
DP3_C2M_P	MGT_TX_P3_117	F2
DP3_C2M_N	MGT_TX_N3_117	F1
DP4_C2M_P	MGT_TX_P0_118	D2
DP4_C2M_N	MGT_TX_N0_118	D1
DP5_C2M_P	MGT_TX_P1_118	C4
DP5_C2M_N	MGT_TX_N1_118	C3

DP6_C2M_P	MGT_TX_P2_118	B2
DP6_C2M_N	MGT_TX_N2_118	B1
DP7_C2M_P	MGT_TX_P3_118	A4
DP7_C2M_N	MGT_TX_N3_118	A3
HA00_P_CC	IO_L14P_SRCC_13	AE28
HA00_N_CC	IO_L14N_SRCC_13	AF28
HA01_P_CC	IO_L13P_SRCC_13	AG29
HA01_N_CC	IO_L13N_SRCC_13	AH29
HA02_P	IO_L24P_13	AJ26
HA02_N	IO_L24N_13	AK26
HA03_P	IO_L22P_13	AH26
HA03_N	IO_L22N_13	AH27
HA04_P	IO_L18P_13	AG30
HA04_N	IO_L18N_13	AH30
HA05_P	IO_L17P_13	AJ28
HA05_N	IO_L17N_13	AJ29
HA06_P	IO_L23P_13	AF26
HA06_N	IO_L23N_13	AF27
HA07_P	IO_L9P_13	AD29
HA07_N	IO_L9N_46	AE29
HA08_P	IO_L5P_13	AA27
HA08_N	IO_L5N_13	AB28
HA09_P	IO_L4P_13	W29
HA09_N	IO_L4N_13	Y29
HA10_P	IO_L20P_13	AJ27
HA10_N	IO_L20N_13	AK28
HA11_P	IO_L21P_13	AG27
HA11_N	IO_L21N_13	AG28
HA12_P	IO_L3P_13	Y28
HA12_N	IO_L3N_13	AA28
HA13_P	IO_L15P_13	AK29
HA13_N	IO_L15N_13	AK30
HA14_P	IO_L16P_13	AE30
HA14_N	IO_L16N_13	AF30
HA15_P	IO_L8P_13	Y30
HA15_N	IO_L8N_13	AA30
HA16_P	IO_L7P_13	AC29
HA16_N	IO_L7N_13	AC30
HA17_P_CC	IO_L11P_SRCC_13	AD27
HA17_N_CC	IO_L11N_SRCC_13	AD28
HA18_P_CC	IO_L12P_MRCC_13	AB27
HA18_N_CC	IO_L12N_MRCC_13	AC27
HA19_P	IO_L19P_13	AC26
HA19_N	IO_L19N_13	AD26
HA20_P	IO_L10P_13	AB29
HA20_N	IO_L10N_13	AB30
HA21_P	IO_L6P_13	AA25

HA21_N	IO_L6N_13	AB25
HA22_P	IO_L2P_13	W27
HA22_N	IO_L2N_13	W28
HA23_P	IO_L1P_13	Y26
HA23_N	IO_L1N_13	AA26
HB00_P_CC	IO_L11P_SRCC_15	L26
HB00_N_CC	IO_L11N_SRCC_15	L27
HB01_P	IO_L22P_15	P21
HB01_N	IO_L22N_15	P22
HB02_P	IO_L6P_15	M20
HB02_N	IO_L6N_15	L20
HB03_P	IO_L3P_15	K23
HB03_N	IO_L3N_15	K24
HB04_P	IO_L19P_15	N19
HB04_N	IO_L19N_15	N20
HB05_P	IO_L24P_15	M22
HB05_N	IO_L24N_15	M23
HB06_P_CC	IO_L12P_SRCC_15	L25
HB06_N_CC	IO_L12N_SRCC_15	K25
HB07_P	IO_L21P_15	P23
HB07_N	IO_L21N_15	N24
HB08_P	IO_L2P_15	L22
HB08_N	IO_L2N_15	L23
HB09_P	IO_L5P_15	J21
HB09_N	IO_L5N_15	J22
HB10_P	IO_L23P_15	M24
HB10_N	IO_L23N_15	M25
HB11_P	IO_L20P_15	N21
HB11_N	IO_L20N_15	N22
HB12_P	IO_L1P_15	J23
HB12_N	IO_L1N_15	J24
HB13_P	IO_L18P_15	N25
HB13_N	IO_L18N_15	N26
HB14_P	IO_L4P_15	L21
HB14_N	IO_L4N_15	K21
HB15_P	IO_L17P_15	N29
HB15_N	IO_L17N_15	N30
HB16_P	IO_L9P_15	L30
HB16_N	IO_L9N_15	K30
HB17_P_CC	IO_L13P_MRCC_15	K28
HB17_N_CC	IO_L13N_MRCC_15	K29
HB18_P	IO_L15P_15	M29
HB18_N	IO_L15N_15	M30
HB19_P	IO_L16P_15	N27
HB19_N	IO_L16N_15	M27
HB20_P	IO_L8P_15	J27
HB20_N	IO_L8N_15	J28

HB21_P	IO_L10P_15	K26
HB21_N	IO_L1N_15	J26



Part 4.16: LEDs

The core board is designed with five LEDs, and the FPGA development board is designed with five LEDs, totaling ten LEDs. The pin location of the LED is shown in the table below. When the pin outputs a high level, the LED lights up, and when the pin outputs a high level, the LED turns off.

LED	FPGA Pin Name	Pin Position
LED1（SOM Core Board)	IO_23P_14	U24
LED2（SOM Core Board)	IO_23N_14	V24
LED3（SOM Core Board)	IO_24P_14	W21
LED4（SOM Core Board)	IO_24N_14	W22
LED5（SOM Core Board)	IO_25_14	W19
LED1 (FPGA Development Board)	IO_L6P_18	L11
LED2 (FPGA Development Board)	IO_L6N_18	K11
LED3 (FPGA Development Board)	IO_L2P_18	L15
LED4 (FPGA Development Board)	IO_L2N_18	K15
LED5 (FPGA Development Board)	IO_L14P_18	F12

Part 4.17: KEYs

The FPGA development board is designed with five-way KEYs. The KEY defaults to a high level, and the KEY is pressed to a low level. The KEY is connected to the PL side, and can also be assigned to the ARM side through EMIO. The pin location of the KEY is as follows:

KYE Number	FPGA Pin Name	Pin Position
KEY 1	IO_L21P_18	D14
KEY 2	IO_L21N_18	C14
KEY 3	IO_L17P_18	A11
KEY 4	IO_L17N_18	A12
KEY 5	IO_L15P_18	C12

Part 4.18: USB to JTAG Interface

One USB to JTAG downloader integrated on the FPGA development board board, after installing the Vivado software, use the USB cable to connect the USB port corresponding to JTAG, you can achieve debugging download, very convenient. The following is the location of the interface on the development board.

