Artix-7 FPGA Board User Manual

CRA35TB / CRA75TB / CRA100TB / CRA200TB

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Version Records:

Data	Version	Description
2019.5.25	V1.0	initial version

This tutorial will continue to revise, optimize and increase based on the actual Experience, that is to provide you with more and better Demos.

If you find some errors or any suggestion, contact with us.

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Part 1: Artix-7 series Introduction

Artix-7 Series: Compared to the Spartan-6 series, the Artix-7 series offers half the power and 35% lower cost in a smaller package and a unified Virtex family architecture to meet the performance requirements of the low-cost, high-volume market, the same market segment previously targeted by ASSPs, ASICs and low-cost FPGAs.

The new product range meets the low-power, high-performance needs of battery-powered portable ultrasound devices, the small, low-power requirements of commercial digital camera lens control, and the stringent SWAP-C (Size, Weight, Power and Cost) of military avionics and communications equipment.

Artix-7 FPGAs

				Transceiver Optimization at the Lowest Cost and Highest DSP Bandwidth (1.0V, 0.95V, 0.9V)							
	Part Number			XC7A12T	XC7A15T	XC7A25T	XC7A35T	XC7A50T	XC7A75T	XC7A100T	XC7A200T
Logic Resources	Logic Cells			12,800	16,640	23,360	33,280	52,160	75,520	101,440	215,360
	Slices			2,000	2,600	3,650	5,200	8,150	11,800	15,850	33,650
	CLB Flip-Flops			16,000	20,800	29,200	41,600	65,200	94,400	126,800	269,200
Memory Resources	Maximum Distributed RAM (Kb)			171	200	313	400	600	892	1,188	2,888
	Block RAM/FIFO w/ ECC (36 Kb each)			20	25	45	50	75	105	135	365
	Total Block RAM (Kb)			720	900	1,620	1,800	2,700	3,780	4,860	13,140
Clock Resources	CMTs (1 MMCM + 1 PLL)			3	5	3	5	5	6	6	10
I/O Resources	Maximum Single-Ended I/O			150	250	150	250	250	300	300	500
	Maximum Differential I/O Pairs			72	120	72	120	120	144	144	240
Embedded Hard IP Resources	DSP Slices			40	45	80	90	120	180	240	740
	PCIe® Gen2[1]			1	1	1	1	1	1	1	1
	Analog Mixed Signal (AMS) / XADC			1	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks			1	1	1	1	1	1	1	1
	GTP Transceivers (6.6 Gb/s Max Rate)[2]			2	4	4	4	4	8	8	16
Speed Grades	Commercial Temp (C)			-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Extended Temp (E)			-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3	-2L, -3
	Industrial Temp (I)			-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L	-1, -2, -1L
	Package[3], [4]	Dimensions (mm)	Ball Pitch (mm)	**Available User I/O**: 3.3V SelectIO™ HR I/O (GTP Transceivers)							
	CPG236	10 x 10	0.5		106 (2)		106 (2)	106 (2)			
	CPG238	10 x 10	0.5	112 (2)		112 (2)					
	CSG324	15 x 15	0.8		210 (0)		210 (0)	210 (0)	210 (0)	210 (0)	
	CSG325	15 x 15	0.8	150 (2)	150 (4)	150 (4)	150 (4)	150 (4)			
	FTG256	17 x 17	1.0		170 (0)		170 (0)	170 (0)	170 (0)	170 (0)	
	SBG484	19 x 19	0.8								285 (4)
Footprint Compatible	FGG484[5]	23 x 23	1.0		250 (4)		250 (4)	250 (4)	285 (4)	285 (4)	
	FBG484[5]	23 x 23	1.0								285 (4)
Footprint Compatible	FGG676[6]	27 x 27	1.0						300 (8)	300 (8)	
	FBG676[6]	27 x 27	1.0								400 (8)
	FFG1156	35 x 35	1.0								500 (16)

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Part 2: Hardware Introduction

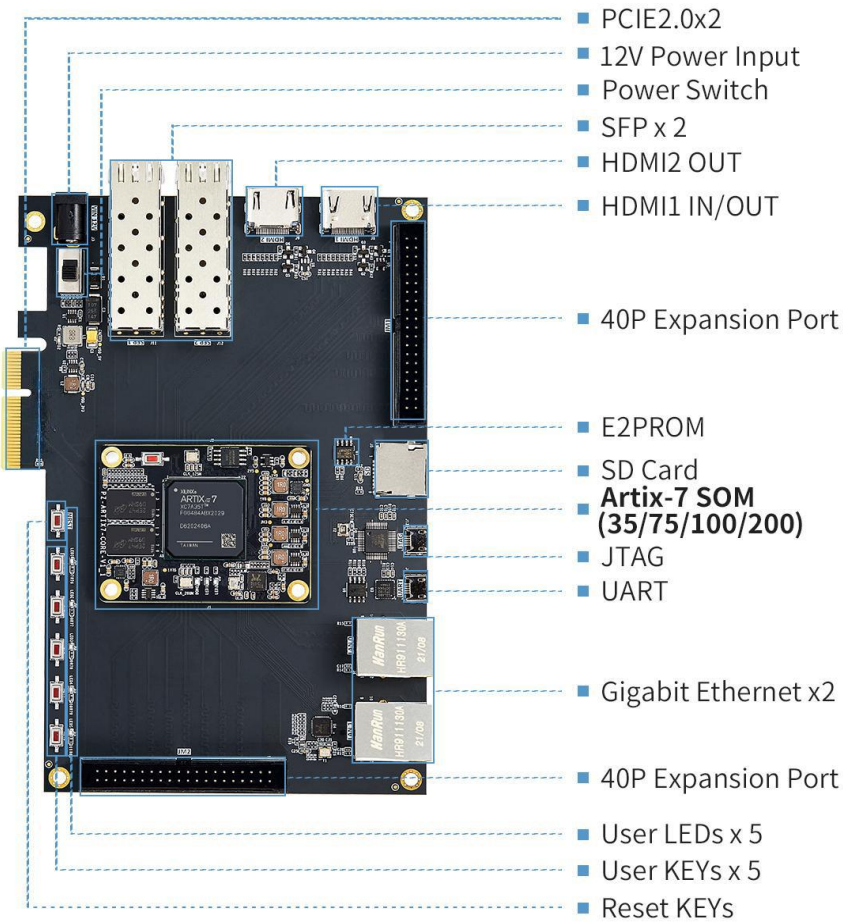
Part 2.1: Board Introduction

The Artix-7 series FPGA development board has four versions, namely CRA735TB 、CRA775TB 、 CRA7100TB и CRA7200TB. The peripherals of the two versions are fully compatible, and the only difference is the logic capacity of the main chip FPGA.

The Artix-7 series FPGA development board adopts the mode of “core board + Carrier board”. The core board plugs into the carrier board connector through four 120P high-speed connectors. More flexible in use. You can use the core board for both learning and project development.

The FPGA development board integrates rich peripheral resources and provides detailed demos. The board also incorporates the JTAG debugger, a MicroUSB cable, and a 12V power supply to get the board working. More convenient for users.

The form factors of the development board is 172 x 116mm. A fixed hole is placed at each of the four corners of the core board for mounting support columns or fixing veneers. The aperture is 3.5mm.

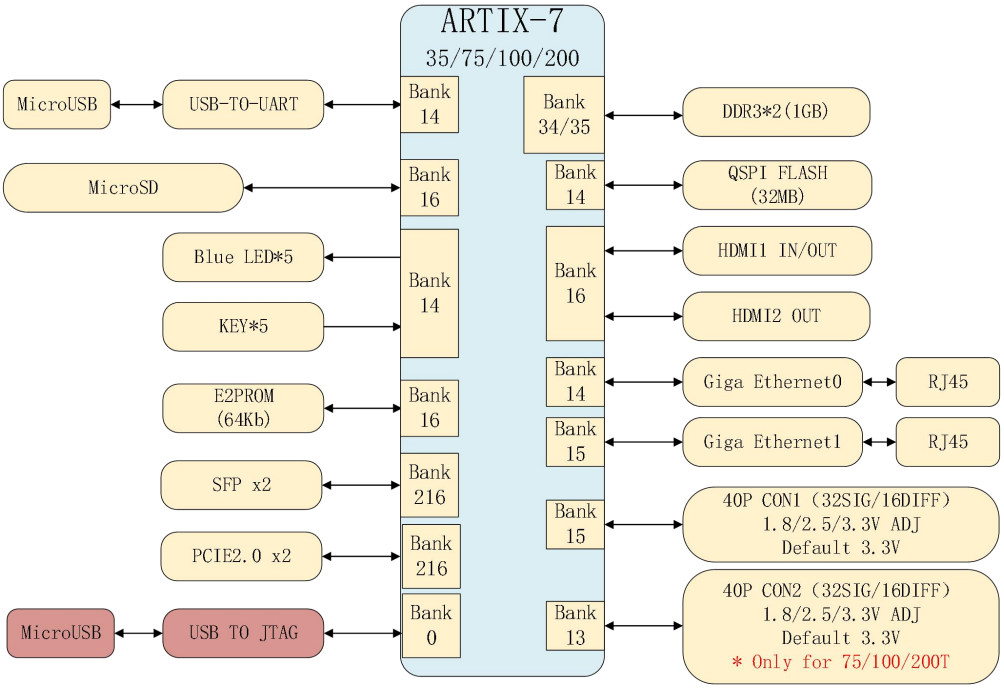


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Part 2.2: FPGA Board Resources and Block Diagram

The onboard resources of the FPGA development board are listed in the table and block diagram below, and the functions we have included can be seen from the table below.

Artix7 FPGA Board Resource				
FPGA Chip	XC7A35T-2FFG484I	XC7A75T-2FFG484I	XC7A100T-2FFG484I	XC7A200T-2FBG484I
Logic Cells	33280	75520	101440	215360
Slices	5200	11800	15850	33650
Block ROM（Kb）	1800	3780	4860	13140
DSP Slices	90	180	240	740
DDR3	1GB（2Pics of 512MByte)			
QSPI FLASH	32MB			
E2PROM	64Kbit			
UART	1			
SD Card	1			
Gigabit Ethernet	1			
HDMI	1 HDMI input and output, 1 HDMI output			
LE,D, Key	2 LEDs (high-level), 5 Keys (low-level)			
PCIE2.0	x 2			
SFP	2			
40P Expansion Port	Total 64 single-ended signals / 32 differential pairs			
Form Factors	172mm x 116mm			
Power Adapter	12V/3A			



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Part 3: SOM Core Board Overview

Part 3.1: SOM Introduction

The ARTIX7 SOM core board adopts the Aritx-7 chip of XILINX company as the main controller. The core board is divided into 35T/75T/100T/200T four models, the chip selection BGA484 package. The core board adopts two 0.6mm pitch 120P gold-plated connectors to connect with the carrier board. Four 3.5mm fixing holes are placed on the four legs of the core board, and this hole can be fastened with the carrier board by screws to ensure stable operation in strong vibration environment.

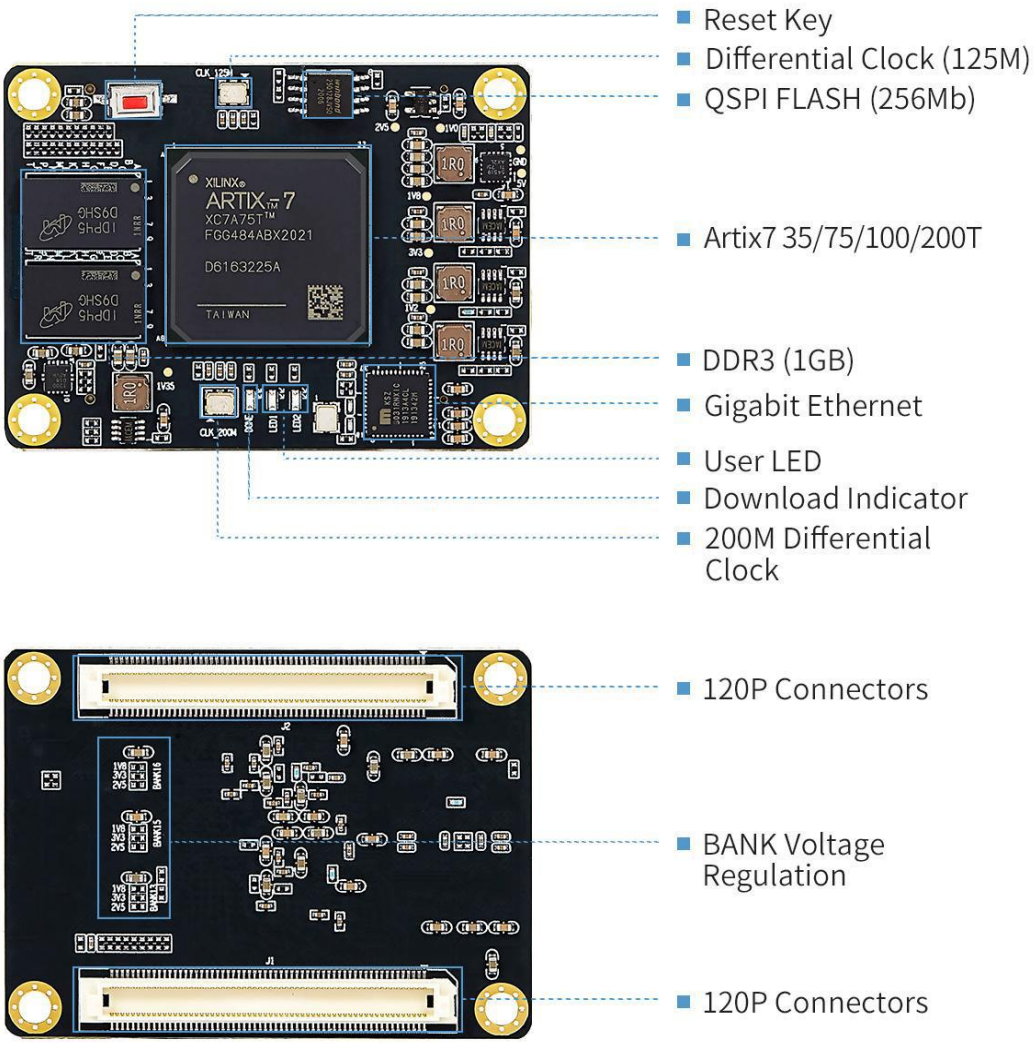
Part 3.2: SOM Specification

Artix7 Industrial Grade SOM Specification				
FPGA Chip	XC7A35T-2FFG484I	XC7A75T-2FFG484I	XC7A100T-2FFG484I	XC7A200T-2FBG484I
Logic Cells	33280	75520	101440	215360
Slices	5200	11800	15850	33650
Block ROM（Kb）	1800	3780	4860	13140
DSP Slices	90	180	240	740
DDR3	1GB（2 Pics of 512MByte）			
QSPI FLASH	32MB			
Start-up Mode	JTAG/QSPI FLASH			
Gigabit Ethernet	1			
User LEDs	2（High Level light, Low Level off）			
Number of IOs	138	172		
Number of GTX ports	1 BANK, 4 Paris of TX/RX each			
Working Voltage/Current	5V/1A			
Working Temperature	-40°C~+85°C			
Connector Height	3mm			

Part 3.3: Product Appearance

As shown in the figure below, the position of each main electronic component on the core board is marked, which is convenient for users to view and identify.

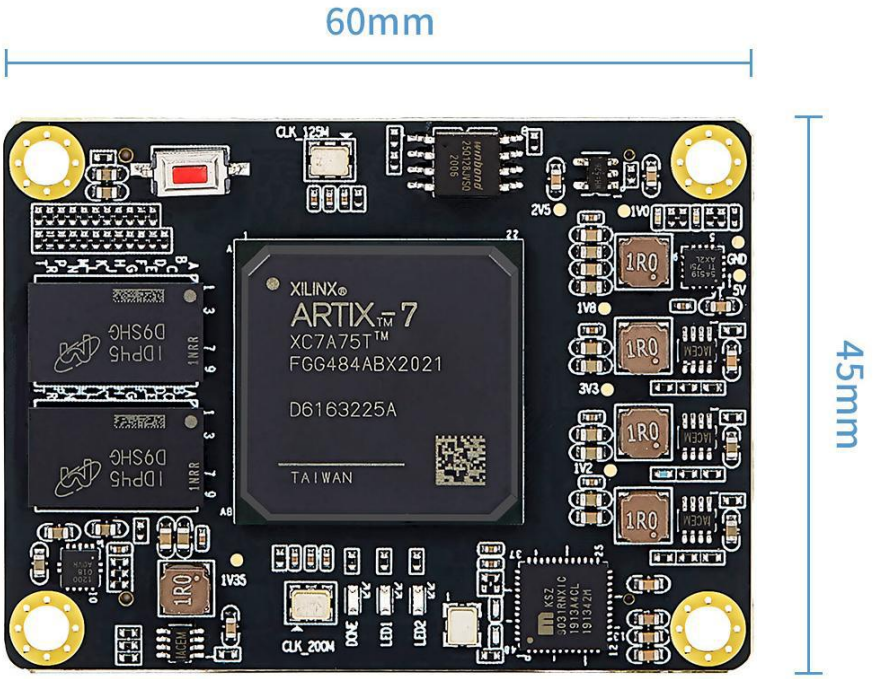
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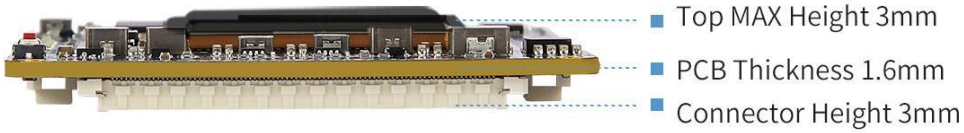


Part 3.4: SOM Form Factors

The Form Factors of the core board is 60 x 45mm. The core board is connected to the Carrier Board through two 0.6mm/120P gold-plated high-speed connectors on the bottom, with a combined height of 3mm. The following figure shows the dimensions of the core board.

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Part 3.5: Power Connection

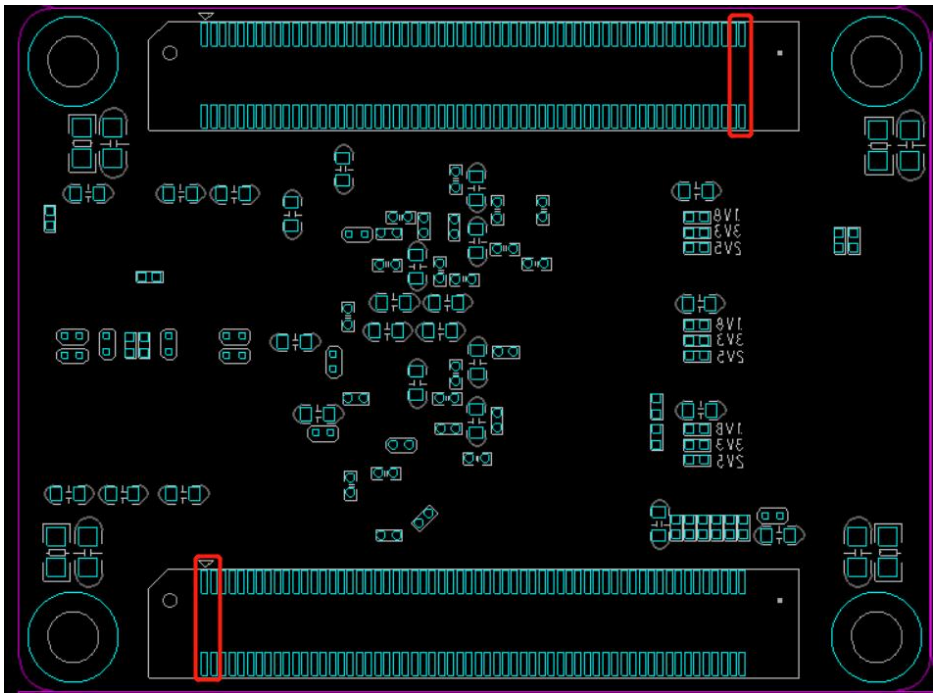
The power supply voltage of the core board is 5V, and the power input pins are reserved in the opposite corners of the core board. The power supply pins have been made connected inside the module, which is designed to facilitate the power access of the carrier board. When designing the carrier board, only one corner of the power supply needs to be connected and the core board can work.

The power connection needs to be connected with copper and enough through holes are made to ensure the power flow capacity. All GND signals on the core board need to be connected to the carrier board, and each GND is connected to the carrier board through two vias. The limit current of the core board power supply is 5V/1.5A, so the external power supply needs to consider the limit current to ensure the stable operation of the core board.

The output voltage of the power supply to the module needs to be stable. Add a first-level DCDC power conversion to the module power input, from high voltage to 5V, and the DCDC current output capacity can be about 5A. For example, you can refer to the power chip MP2482. Two **220uF/25V** capacitors should be placed at the power input of the module to ensure power quality. If the switching frequency of the selected switching power supply is

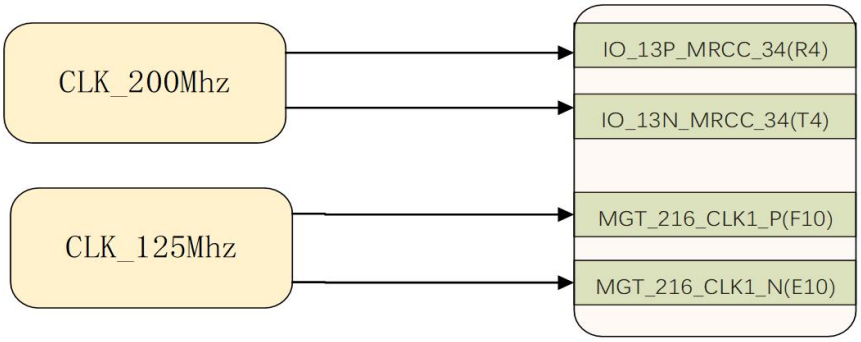
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relatively low, it is necessary to increase the value of the external filter capacitor.



Part 3.2: System Clock

The core board is placed on two active differential crystal, 200M clock for the logic side to provide a differential clock, 125M for the GTX interface to provide a differential clock. The following figure, 200M differential clock to the 13P/13N pin of the BANK34 , the corresponding pin location is R4/T4. 125M clock to F10/E10 of BANK216

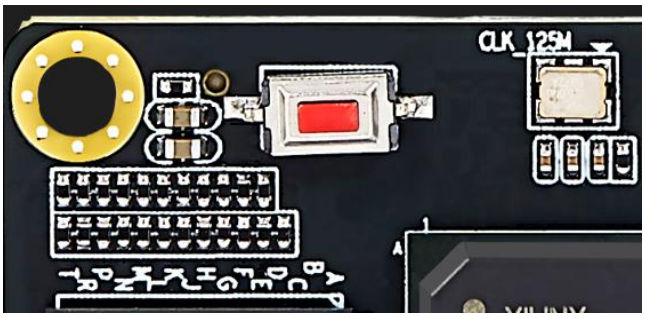


Part 3.7: Global Reset

The Core board reserved a reset key for debugging use, this reset key using RC circuit, reset is not sufficient, only as a debugging use, the key is connected to the FPGA BANK65, the corresponding pin is IO_11N_SRCC_14(V20).

The actual product needs to add a reset circuit, you can use a special reset chip on the carrier board, such as MAX811, or other longer reset time chip.

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Part 3.8: Boot Mode Selection

The core board supports two boot modes, JTAG and QSPI Flash, and the default is QSPI Flash.

BOOT MODE	M2	M1	M0
JTAG	1	0	1
M SPI	0	0	1

Part 3.9: Gigabit Ethernet chip

One Gigabit Ethernet chip is placed on the core board. The Ethernet chip and the ZYNQ chip are interconnected through the RGMII interface. The corresponding pins are shown in the table below. Ethernet external connection only needs an RJ45 with a transformer to use, the chip address PHY_AD[2:0]=001, the connection schematic diagram can refer to the following figure

RMGII0 Signal	Pin Name	Pin Position
TX_CLK	IO_21P_14	N17
TXD0	IO_3N_14	V22
TXD1	IO_7N_14	W22
TXD2	IO_7P_14	W21
TXD3	IO_9N_14	Y22
TX_EN	IO_9P_14	Y21
RX_CLK	IO_11P_14	U20
RXD0	IO_8P_14	AA20
RXD1	IO_10P_14	AB21
RXD2	IO_8N_14	AA21
RXD3	IO_10N_14	AB22

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RX_CTL	IO_15N_14	AB20
PHY_nRST（预留）	IO_21N_14	P17
MDC	IO_15P_14	AA19
MDIO	IO_6N_14	T20

Part 3.10: QSPI FLASH

The FPGA development board has a 32MB QSPI FLASH onboard, the model is MX25L25645GM2I-08G, which can be used to store startup files and user files.



QSPI FLASH Pin	FPGA Pin Name	Pin Position
DATA0	IO_1P_14	P22
DATA1	IO_1N_14	R22
DATA2	IO_2P_14	P21
DATA3	IO_2N_14	R21
QSPI_CS	IO_6P_14	T19
QSPI_CLK	CCLK_0	L12

Part 3.11: On-board LED

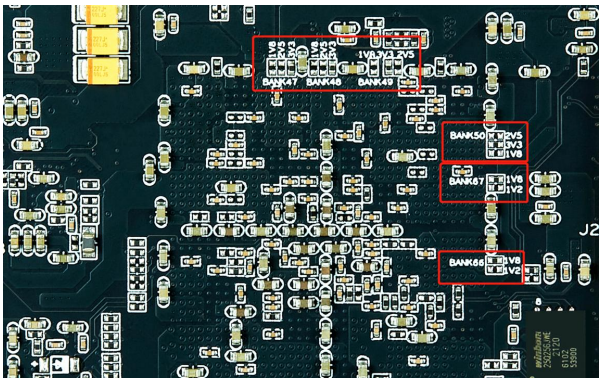
In order to facilitate debugging, two LEDs are placed on the core board. The pin positions of the LEDs are as shown in the table below. When the pin outputs a high level, the LED lights up, and the low level LED goes out.

Number	Pin Name	Pin Position
LED1	IO_0_14	P20
LED2	IO_25_14	N15

Part 3.12: BANK Interface Level Selection

The BANK66/67 on the core board are HP BANK, the interface level is configured as 1.2/1.8V, and the voltage can be adjusted by 0 ohm resistance welding through the instructions provided on the single board, and the default level is 1.8V. BANK47/48/49/50 are HD BANK, BANK level can realize 1.8V/2.5V/3.3V three level conversion, just change the resistor position, the default level is 3.3V.

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Part 3.13: DDR3 Pin Connection

The core board contains two industrial-grade DDR3L chips with a single capacity of 512MB and a total capacity of 1GB. The model is "**MT41K256M16TW-107IT:P**", DDR3L pin allocation see the following table.



DDR3 Pin	FPGA Pin Name	Pin Position
DDR3_D0	IO-L2P-35	C2
DDR3_D1	IO-L5P-35	G1
DDR3_D2	IO-L1N-35	A1
DDR3_D3	IO-L6P-35	F3
DDR3_D4	IO-L2N-35	B2
DDR3_D5	IO-L5N-35	F1
DDR3_D6	IO-L1P-35	B1
DDR3_D7	IO-L4P-35	E2
DDR3_DM0	IO-L4N-35	D2
DDR3_DQS_P0	IO-L3P-35	E1

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DDR3_DQS_N0	IO-L3N-35	D1
DDR3_D8	IO-L11P-35	H3
DDR3_D9	IO-L11N-35	G3
DDR3_D10	IO-L8P-35	H2
DDR3_D11	IO-L10N-35	H5
DDR3_D12	IO-L7N-35	J1
DDR3_D13	IO-L10P-35	J5
DDR3_D14	IO-L7P-35	K1
DDR3_D15	IO-L12P-35	H4
DDR3_DM1	IO-L8N-35	G2
DDR3_DQS_P1	IO-L9P-35	K2
DDR3_DQS_N1	IO-L9N-35	J2
DDR3_D16	IO-L18N-35	L4
DDR3_D17	IO-L16P-35	M3
DDR3_D18	IO-L14P-35	L3
DDR3_D19	IO-L17N-35	J6
DDR3_D20	IO-L14N-35	K3
DDR3_D21	IO-L17P-35	K6
DDR3_D22	IO-L13N-35	J4
DDR3_D23	IO-L18P-35	L5
DDR3_DM2	IO-L16N-35	M2
DDR3_DQS_P2	IO-L15P-35	M1
DDR3_DQS_N2	IO-L15N-35	L1
DDR3_D24	IO-L20N-35	P1
DDR3_D25	IO-L19P-35	N4
DDR3_D26	IO-L20P-35	R1
DDR3_D27	IO-L22N-35	N2
DDR3_D28	IO-L23P-35	M6
DDR3_D29	IO-L24N-35	N5
DDR3_D30	IO-L24P-35	P6
DDR3_D31	IO-L22P-35	P2
DDR3_DM3	IO-L23N-35	M5
DDR3_DQS_P3	IO-L21P-35	P5
DDR3_DQS_N3	IO-L21N-35	P4
DDR3_A0	IO-L11N-34	AA4
DDR3_A1	IO-L8N-34	AB2
DDR3_A2	IO-L10P-34	AA5
DDR3_A3	IO-L10N-34	AB5
DDR3_A4	IO-L7N-34	AB1
DDR3_A5	IO-L6P-34	U3
DDR3_A6	IO-L5P-34	W1
DDR3_A7	IO-L1P-34	T1

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DDR3_A8	IO-L2N-34	V2
DDR3_A9	IO-L2P-34	U2
DDR3_A10	IO-L5N-34	Y1
DDR3_A11	IO-L4P-34	W2
DDR3_A12	IO-L4N-34	Y2
DDR3_A13	IO-L1N-34	U1
DDR3_A14	IO-L15N-34	W5
DDR3_BA0	IO-L9N-34	AA3
DDR3_BA1	IO-L9P-34	Y3
DDR3_BA2	IO-L11P-34	Y4
DDR3_CS	IO-L8P-34	AB3
DDR3_RAS	IO-L12P-34	V4
DDR3_CAS	IO-L12N-34	W4
DDR3_WE	IO-L7P-34	AA1
DDR3_ODT	IO-L14N-34	U5
DDR3_RESET	IO-L15P-34	W6
DDR3_CLK_P	IO-L3P-34	R3
DDR3_CLK_N	IO-L3N-34	R2
DDR3_CKE	IO-L14P-34	T5

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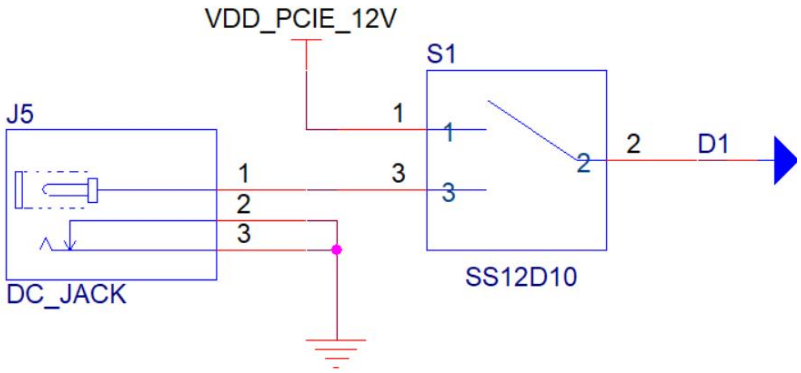
Part 4: Carrier Board Overview

Part 4.1: Power Supply and BANK Voltage Regulation

The FPGA development board provides two power supply modes: PCIE interface and 12V/3A power adapter. The two power supply options can be selected by DIP switch S1 on the FPGA development board. If switch S1 is moved to a position close to the DC005 plug, the external adapter is used for power supply. If switch S1 is moved to the other side, the PCIE interface is powered.

After the 12V power supply enters the FPGA development board, it is converted into 5V/3.3V power supply through the secondary power supply, which is used by the core board and the internal and external peripherals of the board. Detailed circuit can refer to the schematic diagram of the FPGA development board.

In addition, the level of each BANK on the core board can be adjusted by 1.8/2.5/3.3V independently. The default level is 3.3V. If you need to adjust the voltage, you can adjust the resistance corresponding to the BANK. For details, refer to the Core Board user manual.



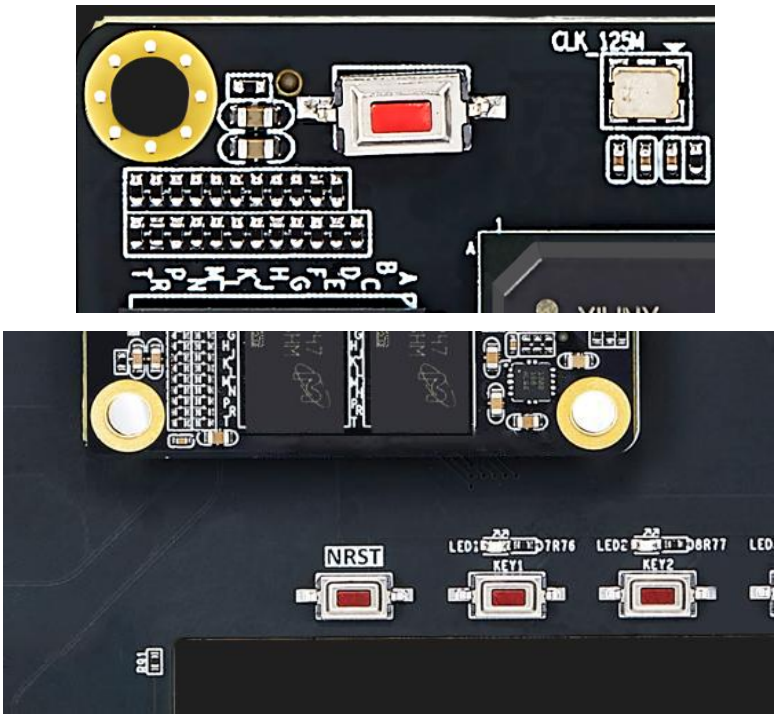
Part 4.2: System Reset

A reset circuit is reserved on the FPGA Carrier board and the SOM core board respectively, the user can choose which one to use according to the actual use.

The reset pin on the core board is connected to BANK14 of the FPGA and the corresponding pin is IO_11N_SRCC_14(V20). The reset pin on the FPGA board is connected to BANK17 of the FPGA and the corresponding pin is IO_9P_14(R14).

If the actual product needs to add reset circuit, you can use a special reset chip on the carrier board, such as MAX811, the user can choose according to the needs.

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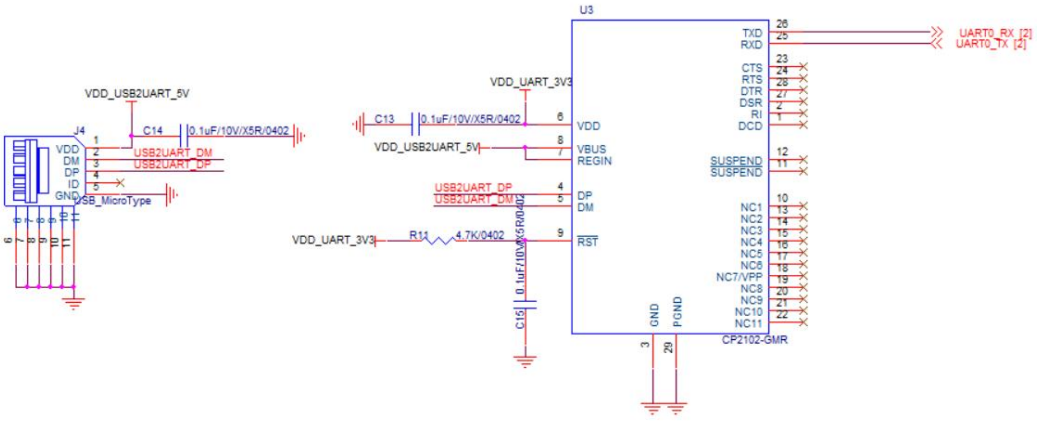


Part 4.3: USB to UART

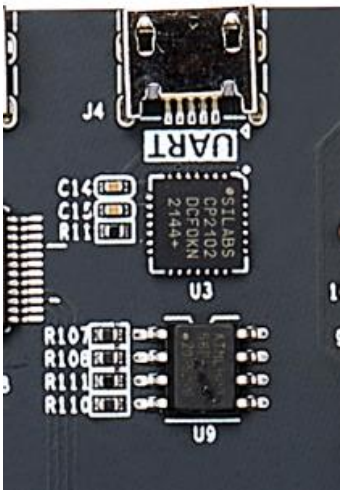
The FPGA development board uses "**Silicon Labs CP2102GM**" chip to realize USB to UART, and the USB interface adopts "**Micro USB**". Users only need to use a Micro USB cable to connect to the PC for serial communication.

The "**TX/RX**" signal of the UART is connected with the "**BANK14**" of the "**FPGA**", and the interface level is 3.3V. The following is the signal correspondence table and schematic diagram, the TX/RX direction is defined on the FPGA side.

UART0 Pin	FPGA Pin Name	Pin Position
UART0_TX	IO-14P-14	V18
UART0_RX	IO-14N-14	V19



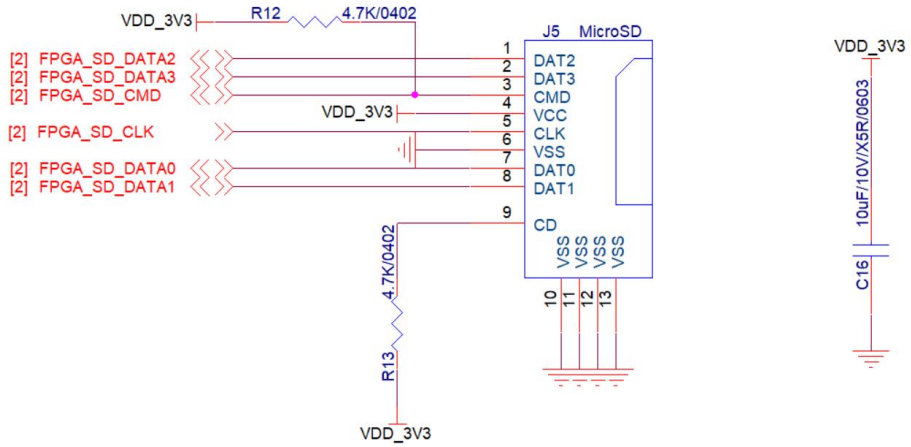
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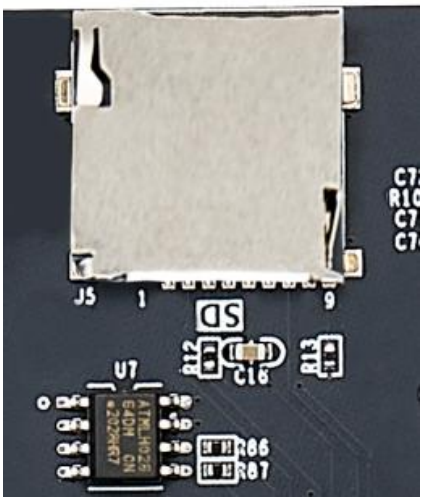
Part 4.4: SD Card

A TF card holder is placed on the FPGA development board, which is convenient for users to store files. The circuit interface level is "**3.3V**", the SD card signal is connected to the "BANK16" of the FPGA. The following is the signal correspondence table and schematic. The TX/RX direction is defined for the FPGA end

SD Card Pin	FPGA Pin Name	Pin Position
SD-CLK	IO-16P-16	B20
SD-CMD	IO-2N-16	E17
SD-DATA0	IO-16N-16	A20
SD-DATA1	IO-21P-16	B21
SD-DATA2	IO-2P-16	F16
SD-DATA3	IO-21N-16	A21



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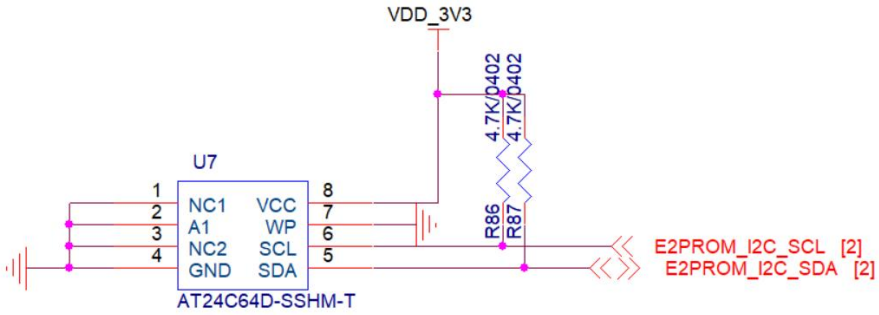


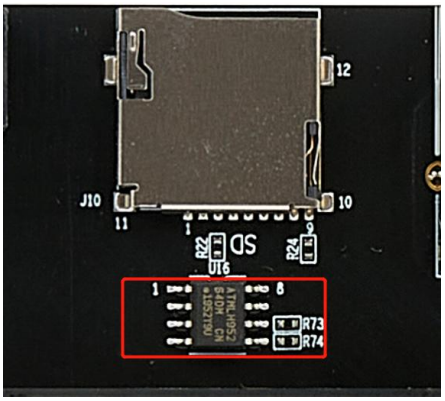
Part 4.5: E2PROM

A 64Kbit EEPROM chip, AT24C64D-SSHM-T, is placed on the FPGA Carrier board, which is connected to BANK16 of FPGA through IIC bus. The read address of EEPROM is 0xA1 and the write address is 0xA0.

The following is the pin assignment and schematic diagram of EEPROM.

EEPROM Pin	FPGA Pin Name	Pin Position
IIC-CLK	IO-23P-16	E21
IIC-DATA	IO-23N-16	D21





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Part 4.6: HDMI Interface

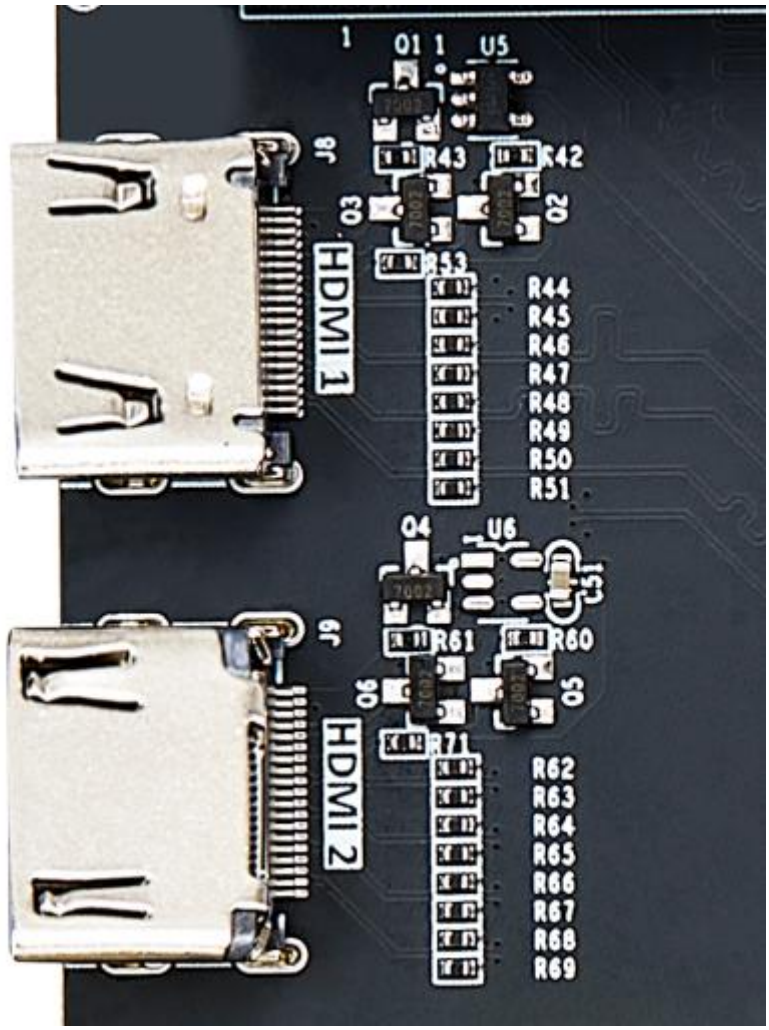
Two HDMI interfaces are placed on the FPGA carrier board, HDMI1 can be used for input and output, HDMI2 can be used for output. The interface signal is connected to BANK16 of the FPGA. For details, please refer to the schematic diagram.

The following is the HDMI pin allocation, the schematic diagram can be viewed in the folder.

HDMI1 Pin	FPGA Pin Name	Pin Position
HDMI1_IIC_SCL	IO-17P-16	A18
HDMI1_IIC_SDA	IO-17N-16	A19
HDMI1_DATA0_P	IO-7P-16	B15
HDMI1_DATA0_N	IO-7N-16	B16
HDMI1_DATA1_P	IO-6P-16	D14
HDMI1_DATA1_N	IO-6N-16	D15
HDMI1_DATA2_P	IO-12P-16	D17
HDMI1_DATA2_N	IO-12N-16	C17
HDMI1_CLK_P	IO-11P-16	B17
HDMI1_CLK_N	IO-11N-16	B18
HDMI1_CEC	IO-18P-16	F19
HDMI1_HPD	IO-19P-16	D20
HDMI1_OUT_EN	IO-19N-16	C20

HDMI2 Pin	FPGA Pin Name	Pin Position
HDMI2_IIC_SCL	IO-8P-16	C13
HDMI2_IIC_SDA	IO-8N-16	B13
HDMI2_DATA0_P	IO-1P-16	F13
HDMI2_DATA0_N	IO-1N-16	F14
HDMI2_DATA1_P	IO-4P-16	E13
HDMI2_DATA1_N	IO-4N-16	E14
HDMI2_DATA2_P	IO-13P-16	C18
HDMI2_DATA2_N	IO-13N-16	C19
HDMI2_CLK_P	IO-14P-16	E19
HDMI2_CLK_N	IO-14N-16	D19
HDMI2_CEC	IO-20P-16	C22
HDMI2_HPD	IO-3P-16	C14
HDMI2_OUT_EN	IO-3N-16	C15

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Part 4.7: Gigabit Ethernet

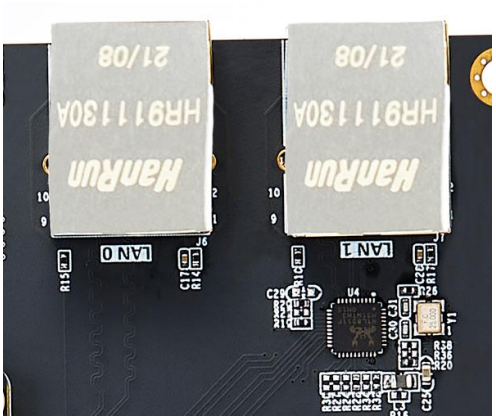
Two Gigabit Ethernet chips are placed on the FPGA development board. One has been integrated into the core board and the other is placed on the carrier board. The Ethernet chip and the FPGA chip are interconnected through the RGMII interface.

PHY0 chip address PHY_AD[2:0]=001, refer to the following table for signal connection. And the Ethernet chip address is **PHY_AD[2:0]=001** in the FPGA Board. There is no ESD protection circuit in reference circuit, and the ESD protection needs to be added to the actual product circuit.

RMGII0 Signal	Pin Name	Pin Position
TX_CLK	IO_21P_14	N17
TXD0	IO_3N_14	V22
TXD1	IO_7N_14	W22
TXD2	IO_7P_14	W21
TXD3	IO_9N_14	Y22
TX_EN	IO_9P_14	Y21
RX_CLK	IO_11P_14	U20

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RXD0	IO_8P_14	AA20
RXD1	IO_10P_14	AB21
RXD2	IO_8N_14	AA21
RXD3	IO_10N_14	AB22
RX_CTL	IO_15N_14	AB20
PHY_nRST（预留）	IO_21N_14	P17
MDC	IO_15P_14	AA19
MDIO	IO_6N_14	T20
RMGII1 Signal	**Pin Name**	**Pin Position**
TX_CLK	IO_24P_15	M15
TXD0	IO_19P _15	K13
TXD1	IO_19N _15	K14
TXD2	IO_22P_15	L14
TXD3	IO_22N_15	L15
TX_EN	IO_24N_15	M16
RX_CLK	IO_12P_MRCC_15	J19
RXD0	IO_3P_15	J14
RXD1	IO_3N_15	H14
RXD2	IO_11P_15	J20
RXD3	IO_11N_15	J21
RX_CTL	IO_12N_15	H19
PHY_nRST	IO_20N_15	L13
MDC	IO_21P_15	K17
MDIO	IO_21N_15	J17



Part 4.8: SFP Interface

Two SFP interfaces are designed on the FPGA development board, and the interface signals are connected with BANK16/BANK216 of FPGA. For details, please refer to the schematic diagram.

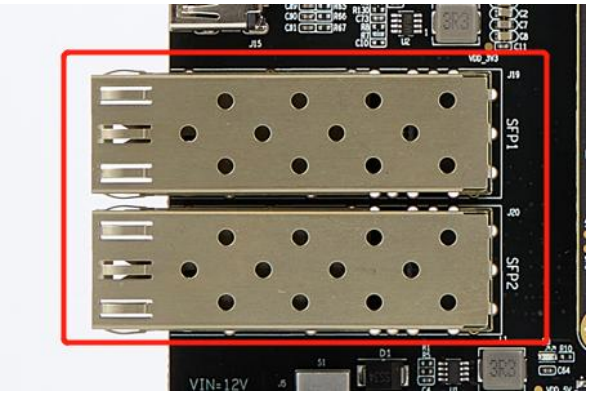
The following is the pin distribution of SFP. The schematic diagram can be viewed in the folder.

SFP1 Pin	FPGA Pin Name	Pin Position

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SFP-TX-P1	MGT-TX-P2-216	B6
SFP-TX-N1	MGT-TX-N2-216	A6
SFP-RX-P1	MGT-RX-P2-216	B10
SFP-RX-N1	MGT-RX-N2-216	A10
SFP1-TX-DISABLE	IO-10N-16	A14

SFP2 Pin	FPGA Pin Name	Pin Position
SFP-TX-P2	MGT-TX-P3-216	D7
SFP-TX-N2	MGT-TX-N3-216	C7
SFP-RX-P2	MGT-RX-P3-216	D9
SFP-RX-N2	MGT-RX-N3-216	C9
SFP2-TX-DISABLE	IO-9P-16	A15

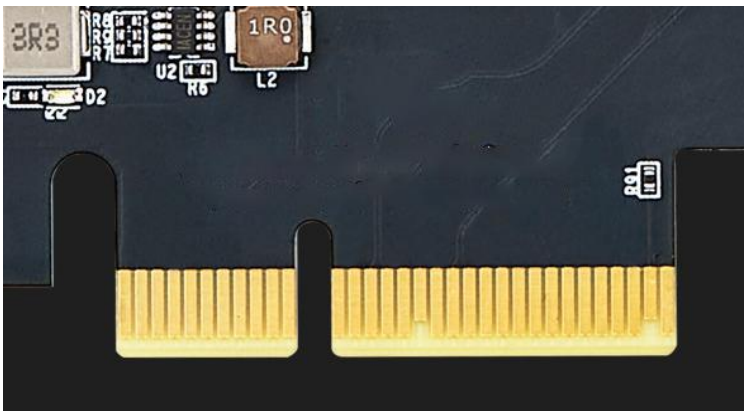


Part 4.9: PCIE Interface

The PCIE2.0 x 2 interface is designed on the FPGA development board, and the interface signal is connected with BANK16/BANK216 of FPGA. The detailed schematic diagram can be referred to.

Signal	FPGA Pin Name	Pin Position
PERST_N	IO_10P_16	A13
REF_CLK_P	MGT_216_CLK_P0	F6
REF_CLK_N	MGT_216_CLK_N0	E6
PER0_P	MGT_216_TX_P1	D5
PER0_N	MGT_216_TX_N1	C5
PER1_P	MGT_216_TX_P0	B4
PER1_N	MGT_216_TX_N0	A4
PET0_P	MGT_216_RX_P1	D11
PET0_N	MGT_216_RX_N1	C11
PET1_P	MGT_216_RX_P0	B8
PET1_N	MGT_216_RX_N0	A8

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Part 4.10: 40P Expansion Ports

The FPGA development board is equipped with two simple 40P 2.54mm pitch horn holders for extended signal connection. The signal is connected to the BANK15/16 of the FPGA, the level can be adjusted to 1.8/2.5/3.3V, the default is 3.3V, if you need to modify the level, you need to find the corresponding BANK adjustment resistor on the core board, and the modification can be achieved. The following table indicates the location of the chip where the signal is located, and the detailed connection relationship reference schematic part.

JM1 Signal	Pin Name	Pin Position	JM2 Signal	Pin Name	Pin Position
5	IO_L4P_15	G17	5	IO_L1P_13	Y16
7	IO_L4N_15	G18	7	IO_L1N_13	AA16
9	IO_L2P_15	G15	9	IO_L16P_13	W15
11	IO_L2N_15	G16	11	IO_L16N_13	W16
13	IO_L6P_15	H17	13	IO_L2P_13	AB16
15	IO_L6N_15	H18	15	IO_L2N_13	AB17
17	IO_L7P_15	J22	17	IO_L6P_13	W14
19	IO_L7N_15	H22	19	IO_L6N_13	Y14
21	IO_L1P_15	H13	21	IO_L4P_13	AA15
23	IO_L1N_15	G13	23	IO_L4N_13	AB15
25	IO_L9P_15	K21	25	IO_L3P_13	AA13
27	IO_L9N_15	K22	27	IO_L3N_13	AB13
29	IO_L23P_15	L16	29	IO_L7P_13	AB11
31	IO_L23N_15	K16	31	IO_L7N_13	AB12
37	IO_L16P_15	M18	37	IO_L8P_13	AA9
39	IO_L16N_15	L18	39	IO_L8N_13	AB10
6	IO_L5P_15	J15	6	IO_L15P_13	T14
8	IO_L5N_15	H15	8	IO_L15N_13	T15
10	IO_L13P_15	K18	10	IO_L14P_13	U15
12	IO_L13N_15	K19	12	IO_L14N_13	V15
14	IO_L8P_15	H20	14	IO_L13P_13	V13

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16	IO_L8N_15	G20	16	IO_L13N_13	V14
18	IO_L10P_15	M21	18	IO_L12P_13	W11
20	IO_L10N_15	L21	20	IO_L12N_13	W12
22	IO_L14P_15	L19	22	IO_L5P_13	Y13
24	IO_L14N_15	L20	24	IO_L5N_13	AA14
26	IO_L15P_15	N22	26	IO_L9P_13	AA10
28	IO_L15N_15	M22	28	IO_L9N_13	AA11
30	IO_L18P_15	N20	30	IO_L11P_13	Y11
32	IO_L18N_15	M20	32	IO_L11N_13	Y12
38	IO_L17P_15	N18	38	IO_L10P_13	V10
40	IO_L17N_15	N19	40	IO_L10N_13	W10

Part 4.11: LEDs

The core board is designed with two LEDs, and the FPGA development board is designed with five LEDs, totaling seven LEDs. The pin location of the LED is shown in the table below. When the pin outputs a high level, the LED lights up, and when the pin outputs a high level, the LED turns off.

LED	FPGA Pin Name	Pin Position
LED1（SOM Core Board）	IO_0_14	P20
LED2（SOM Core Board）	IO_25_14	N15
LED1（FPGA Development Board）	IO-L22P -14	P15
LED2（FPGA Development Board）	IO-L22N -14	R16
LED3（FPGA Development Board）	IO-L23P -14	N13
LED4（FPGA Development Board）	IO-L23N -14	N14
LED5（FPGA Development Board）	IO-L17P -14	AA18

Part 4.12: KEYs

The FPGA development board is designed with five-way KEYs. The KEY defaults to a high level, and the KEY is pressed to a low level. The KEY is connected to the PL side, and can also be assigned to the ARM side through EMIO. The pin location of the KEY is as follows:

KYE Number	FPGA Pin Name	Pin Position
KEY 1	IO-L17N-14	AB18
KEY 2	IO-L13P-14	Y18
KEY 3	IO-L13N-14	Y19
KEY 4	IO-L18P-14	U17
KEY 5	IO-L18N-14	U17

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