# ZYNQ 7000 7035/7045/7100 FPGA Development Manual



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# Version Records:

| Data | Version | Description |
|---|---|---|
| 2019.5.25 | V1.0 | initial version |
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| | | |

This tutorial will continue to revise, optimize and increase based on the actual Experience, that is to provide you with more and better Demos.

If you find some errors or any suggestion, contact with us.

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# Part 1: ZYNQ Introduction

The Zynq family is the industry's first scalable processing platform from Xilinx. Designed to provide the level of processing and computing performance required for high-end embedded applications such as video surveillance, automotive driver assistance, and factory automation.

✓ **Origin of the name ZNYQ**

The word Zynq is easily reminiscent of zinc, the chemical element most commonly found in batteries, sunscreens, alloys, and pharmaceuticals. Alloys of zinc with other metals can achieve enhanced functionality, showing different colors depending on the object of the alloy. The most common use of zinc is in electroplating, so how does the name relate to electroplating?

At the Embedded Systems Conference held in Silicon Valley in April 2010, Xilinx released the architectural details of the scalable processing platform. This SoC based on the ubiquitous ARM processor can meet the high-performance, low-cost requirements of complex embedded systems. Power consumption and multi-core processing power requirements. The core essence of Xilinx's scalable processing platform chip hardware is to use the universal basic dual ARM Cortex-A9MPCore processor system as the "main system", combined with low-power 28nm process technology, to achieve a high degree of flexibility, powerful configuration functions and high performance. performance. Since the programmable logic part of this new device is based on Xilinx 28nm7 series FPGA, "7000" is added to the name of this series of products to maintain consistency with the 7 series FPGA, and also to facilitate the naming of new products in this series in the future .

In addition to the chips, the Xilinx Zynq-7000 family also forms the basis for the final platform offering. The software development and hardware design implementation tools, widely adopted operating systems, debuggers, IP, and other elements provided by members of the Xilinx Alliance Program ecosystem and the ARM Connected Community are "plated" together, making it possible to It is possible to expand the processing platform.

✓ **Why is the Zynq-7000 not an FPGA?**

The Zynq-7000 scalable processing platform is the latest in a family of products using the same 28nm programmable technology used in Xilinx's next-generation FPGAs (Artix-7 and Kintex-7 FPGAs). Programmable logic can be configured by the user and connected together by "interconnect" modules, which can provide user-defined arbitrary logic functions, thereby extending the performance and functionality of the processing system. However, unlike FPGAs with embedded processors, processing systems in the Zynq-7000 product family not only start at power-on, but also configure programmable logic as needed. With this approach, the software programming model is identical to a full-featured standard ARM processing SoC.



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✓ **What does "Scalable" mean?**

In the field of software engineering, scalability (sometimes confused with forward compatibility) refers to the principles of system design in which implementations take into account future development needs. It's a systemic move that can scale the system, and it's the work that's needed to scale. An extension can be embodied as the addition of new functionality or as a modification of existing functionality. Its core theme is to implement changes while minimizing changes to existing system functions. In system architecture, extensibility means that the system is designed to include mechanisms and hooks to extend/improve itself with new functionality without major modifications to the system infrastructure. A good architecture reflects the design principles to achieve the above and also provides a roadmap for possible future builds. Note that this usually means that the final product shipped contains features and mechanisms that will not (in fact probably never will) be used yet, but are not optional, but maintainability Essential elements that help avoid premature obsolescence of products.

✓ **ZYNQ = Processor**

Each product of the Zynq-7000 embedded processing platform series adopts a dual-core ARMCortex-A9MPCore processing system with NEON and double-precision floating-point engine. The system is fully integrated including L1, L2 cache, memory controller and common peripherals through hard wiring. The processing system can not only start and run various operating systems (OS) independent of the programmable logic at boot time, but also configure the programmable logic as required. With this approach, the software programming mode is identical to a full-featured standard ARM processing SoC.

Application developers can take advantage of the powerful parallel processing capabilities of programmable logic to not only solve large-scale data processing problems in many different signal processing applications, but also to extend the characteristics of the processing system by implementing additional peripherals. The high-bandwidth AMBA®-AXI interconnect between the system and programmable logic supports gigabit-level data transfers at very low power consumption, solving common performance bottlenecks between control, data, I/O and memory.

✓ **Programming Environment**

The Zynq-7000 family provides an open design environment that facilitates parallel development of dual-core Cortex-A9MPCore and custom accelerators in programmable logic, accelerating time-to-market. Software developers can take advantage of the Eclipse-based XilinxPlatformStudio Software Development Kit (SDK), ARM's DS-5 and ARMRealViewDesignSuite (RVDS), or leading players in the ARM Connected Community and Xilinx Alliance Program ecosystems such as Lauterbach, WindRiver, PetaLogix , MathWorks, MentorGraphics, Micrium and MontaVista, etc.) provide compilers, debuggers and applications.

In addition, taking advantage of Xilinx's award-winning ISE® Design Suite, the programmable fabric of the Zynq-7000 family can be tailored to maximize system-level performance to meet the diverse needs of specific applications. The kit provides a complete



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hardware development environment including development tools, AMB4AXI4 plug-and-play IP cores, and bus functional models (BFMs) to help accelerate design and verification efforts. Xilinx has further advanced its progress in tools with the acquisition of AutoESL, a leader in advanced synthesis technology, to provide C, C++ and System C synthesis optimized for the Zynq-7000 device architecture. Future releases will also facilitate the seamless transition of key algorithms between processors and programmable logic in the Zynq-7000 product family.

Over time, the above solutions will be further expanded by third-party vendors in the ARM Connected Community and the Xilinx Alliance Program ecosystem, which is part of the Xilinx Targeted Design Platform that provides IP cores, reference designs, development kits and other resources, etc., to meet the requirements of specific applications and design areas.

✓ **Programmable Logic Architecture**

The programmable logic of the Zynq-7000 series is completely designed based on Xilinx's latest 7 series FPGA architecture, which ensures that the IP cores, tools and performance of the 28nm series devices are 100% compatible. The smallest Zynq-7000, Zynq-7010 and Zynq-7020 are based on the Artix-7 family optimized for low cost and low power consumption; the larger Zynq-7030 and Zynq-7040 devices are based on including 4 to 12 10.3Gbps Transceiver channel for mid-range Kintex-7 family supporting high-speed off-chip connectivity. All four products feature a new analog mixed-signal module based on two 12-bit 1Msps ADC (analog-to-digital converter) modules.



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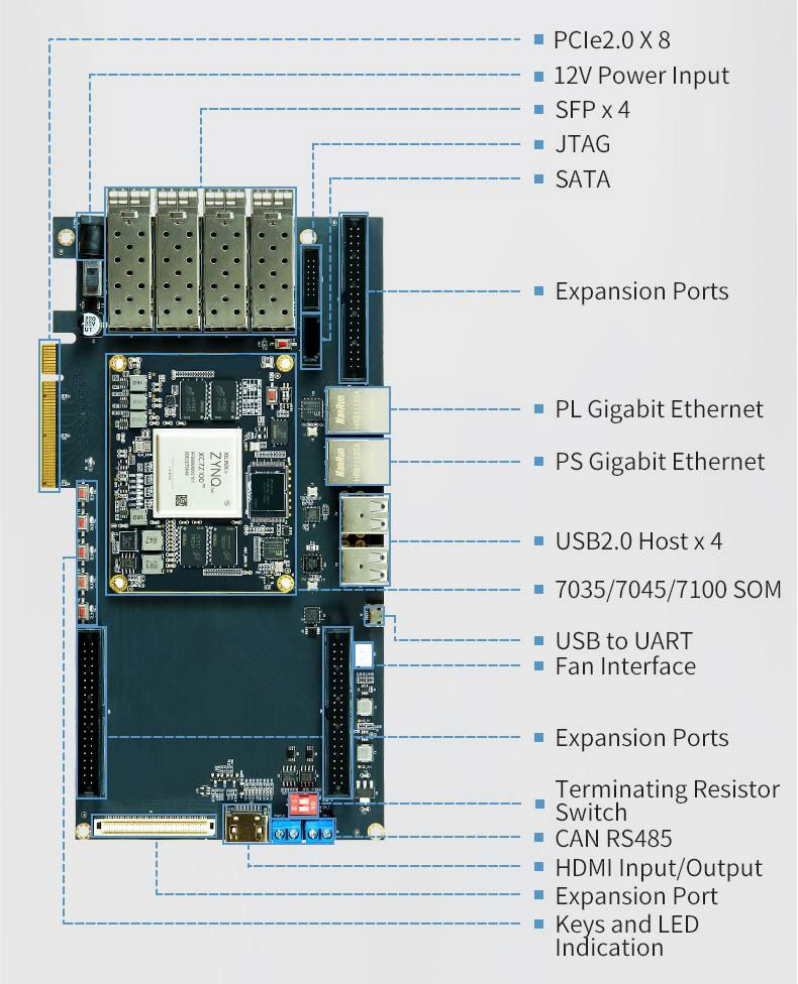
# Part 2: FPGA Development Board Overview

## Part 2.1: Board Introduction

The CR7035/CR7045/CR7100 FPGA development board adopts the mode of "core board + Carrier board". The ZYNQ 7000 Family FPGA Development Boards respectively using XC7Z035-2FFG900I,XC7Z045-2FFG900I and XC7Z100-2FFG900I chips from XILINX as the main controller. The FPGA development board integrates a wealth of peripheral resources and provides detailed development routines to facilitate the use and verification of users.

The Form Factors of the FPGA development board is 220 x 116mm, and a fixing hole is placed at each of the four corners of the board to install the support column or fix the board, and the hole diameter is 3.5mm.



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# Part 2.2: FPGA Board Resources and Block Diagram

The onboard resources of the FPGA development board are listed in the table and block diagram below, and the functions we have included can be seen from the table below.

| CR7035B/ CR7045B/ CR7100B FPGA Board Resource | | | |
|---|---|---|---|
| FPGA | XC7Z035-2FFG900I | XC7Z045-2FFG900I | XC7Z100-2FFG900I |
| DDR3 | PS:1GB/PL:1GB | | |
| EMMC | 8GB | | |
| QSPI FLASH | 32MB | | |
| E2PROM | 64Kbit | | |
| UART/RS485/CAN | 1/1/1 | | |
| SD Card | 1 | | |
| USB1.0 Host/Slave | 1/1 | | |
| Gigabit Ethernet | 2 | | |
| HDMI | 1 channel HDMI Output | | |
| LED, Keys | 5-way LEDs (high-level), 5-way Keys (low-level) | | |
| SATA | 1 | | |
| PCIE2.0 | x 8 | | |
| SFP | 4 | | |
| 40P Expansion Ports | 3 * 40P Expansion Ports, 96 single-ended signals/48 pairs of differential signals | | |
| 120P Expansion Ports | 1 * 120P Expansion Ports, 76 single-ended signals/38 pairs of differential signals | | |



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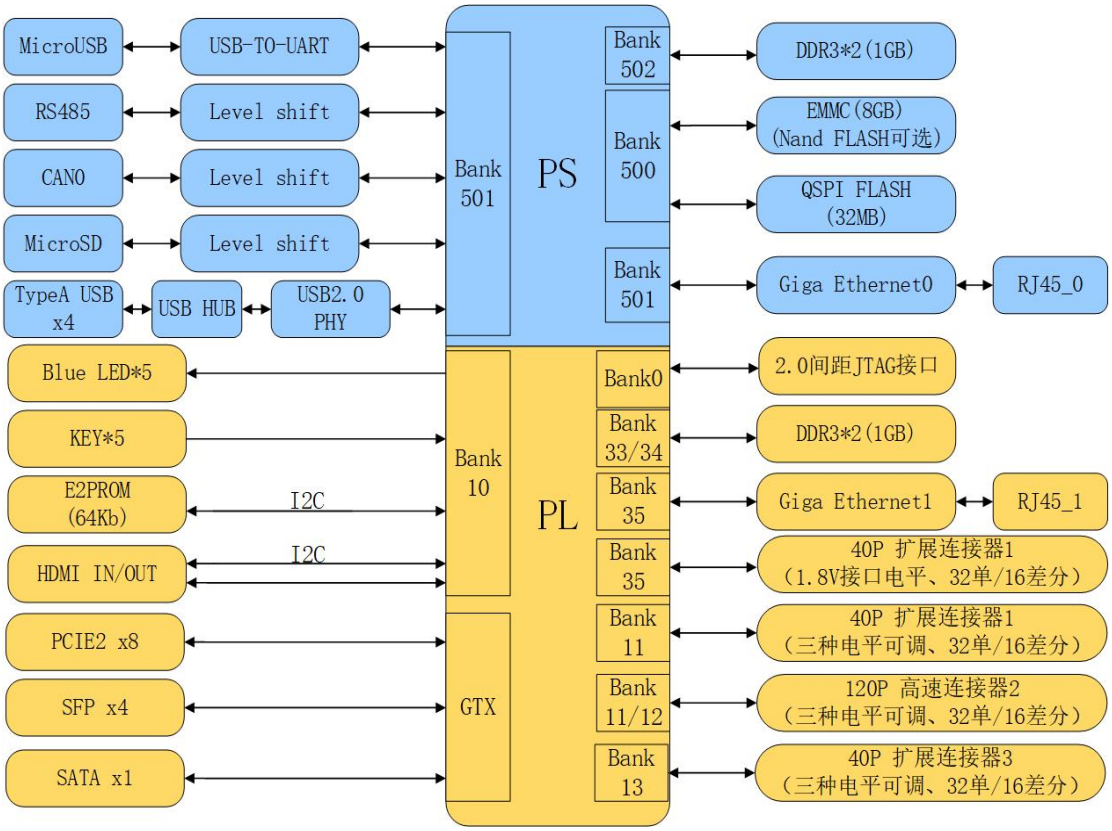




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# Part 3: SOM FPGA Core Board

## Part 3.1: SOM Introduction

The CR7035/45/100 core board adopts XILINX's Zynq7035/7045/7100 chip as the main controller. The core board is connected with the carrier board by four gold-plated connectors with a spacing of 0.6mm and 120P. Four 3.5mm fixing holes are placed on the four feet of the core board, which can be fastened with the carrier board by screws. To ensure stable operation in the environment of strong vibration, in addition, the core board uses industrial grade components, stable operation from -40°C to +85°C.

## Part 3.2: SOM Specification

| **CR7035C/CR7045C/CR7100C Industrial Grade SOM Specification** | | | |
|---|---|---|---|
| FPGA | XC7Z035-2FFG900I | XC7Z045-2FFG900I | XC7Z100-2FFG900I |
| Processor Core | Dual-Core ARM Cortex-A9, Main Frequency 800Mhzz | | |
| Logic Cells | 275K | 350K | 444K |
| Look-up Tables（LUTs） | 171900 | 218600 | 277400 |
| Flip-Flops | 343800 | 437200 | 554800 |
| DSP Slices | 900 | 900 | 2020 |
| Block RAM | 17.6Mb | 19.2Mb | 26.5Mb |
| DDR3/DD3L | PS-side 1GB, PL-side 1GB | | |
| QSPI FLASH | 32Mb, to store startup files and user files | | |
| EMMC | 8GB, to store startup files and user files | | |
| NAND FALSH | 4GB, either NAND FALSH or EMMC<br>The default is EMMC, which stores startup and user files | | |
| Start Method | JTAG/QSPI/NAND/SD, onboard DIP switch selection | | |
| Gigabit Ethernet | 1 （PS Side） | | |
| User LED | 5 | | |
| IO Number | 24 PS Ports (level fixed 1.8V), 240 PL Ports<br>(48 IO level fixed 1.8V; 192 IO level 1.8/2.5/3.3 adjustable) | | |
| Number of GTX ports | BANK, 16 Paris of TX/RX each | | |
| Working Voltage/Max. Current | 8-12V/2A (8V recommended) | | |
| Working Temperature | -40°C~+85°C | | |
| Form Factors<br>Technology | 83.8x63.8mm, Immersion Gold Process<br>0.6mm 120P Connectors X 4 | | |
| Connectors Height | 3mm | | |



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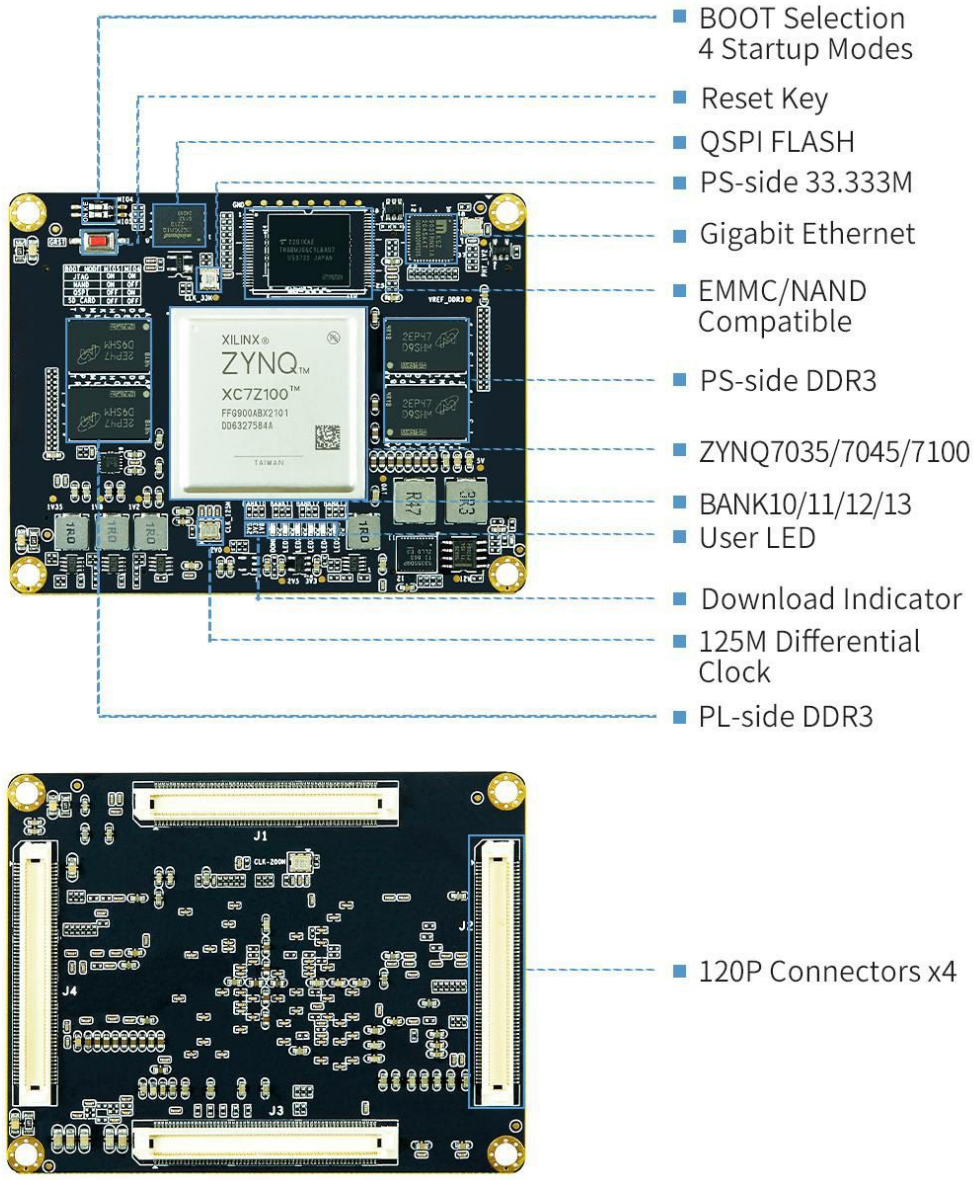
# Part 3.3: Product Appearance

The following figure shows the location of each major electronic component on the core board for easy identification.



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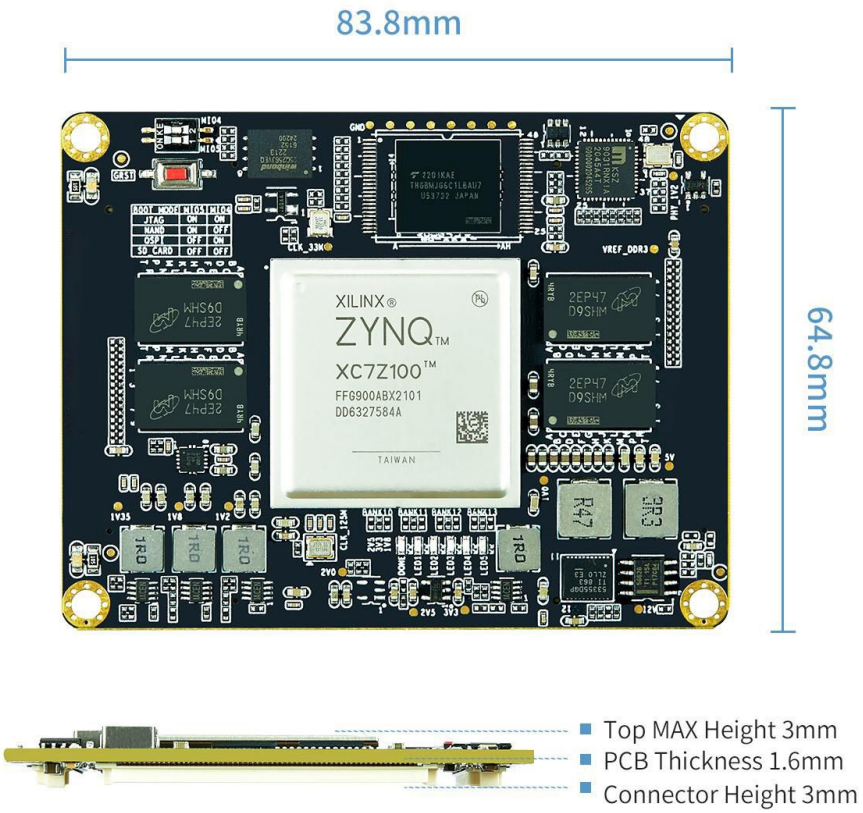
## Part 3.4: SOM Form Factors

The core board size is 83.8 mm x 64.8mm. The core board is connected to the carrier board via four 0.6mm/120P gold-plated high-speed connectors on the bottom.




## Part 3.5: Power Connection

The power supply voltage range of the FPGA core board is 7-12V. The Power input pins are reserved at the four corners of the module, and the power pins have been connected inside the module. When designed, it only needs to connect the power pin core board at one corner to work. The power connection needs to be connected with copper and enough holes are made to ensure the power flow ability. All GND signals on the module need to be connected to the base plate, and each GND is connected to the carrier board through two through-holes to ensure through-flow capability.

The output voltage of the power supply supplying the module needs to be stable. If the power supply is unstable, one stage of DCDC should be added before the input of the



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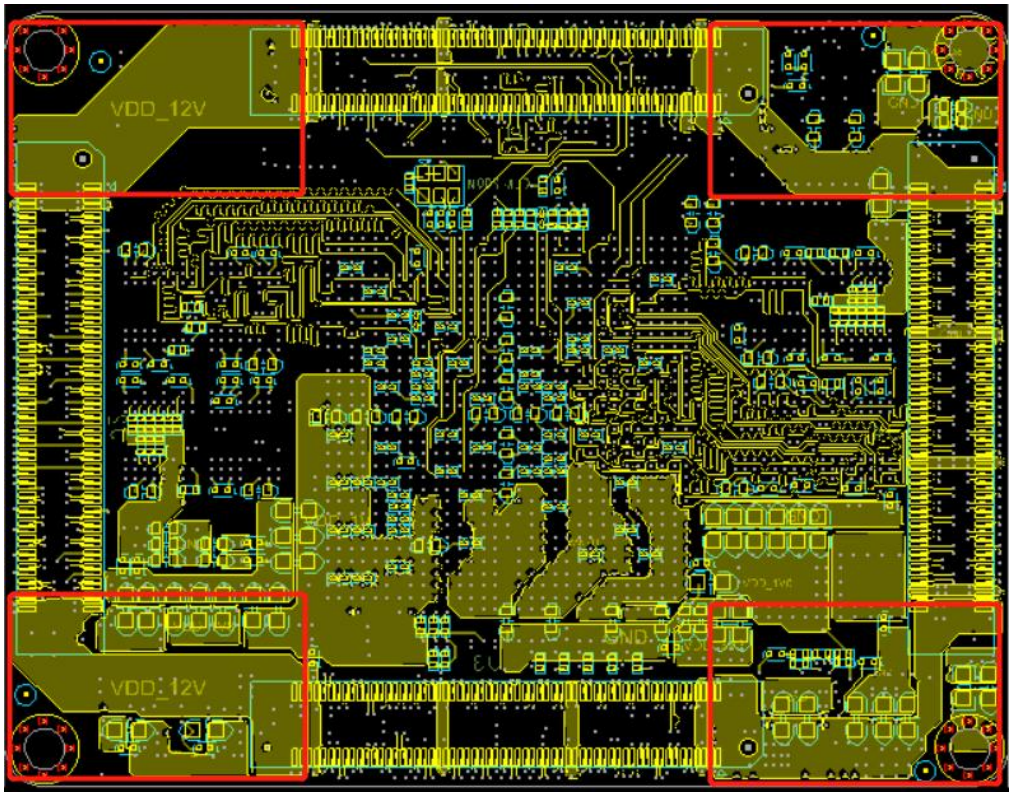
module power supply to switch from high voltage to low voltage. The current output capacity of DCDC can be about 4A.

Two **220uF/ 25V-470uF /25V** capacitors should be placed in the power input of the core board to ensure the quality of the power supply. Since the current of the core board is relatively large, it is recommended to use DCDC power supply alone for the core board if the cost permits, and use another power supply for other peripherals. The power supply should be separated.




## Part 3.6: System Clock

The core board provides a clock input of 33.333333Mhz for the PS side, and the input pin position is PS_CLK_500. A 200Mhz differential clock input is provided for the PL side. The clock input pin of the PL side is FPGA_13P_MRCC_34/FPGA_13N_MRCC_34, and the pin position is H9/G9. A 125Mhz differential clock input is provided for GTX, the input position is CLK1 of BANK110 GTX, and the pin number is AC8/AC7. The connection mode is listed in the following figure.

Note that the GTX CLK on the core board can be used to Bank109/110/111

If BANK112 is used, it is necessary to add a differential 125M clock on the carrier board, you can refer to the FPGA development board schematic diagram connected to the clock circuit of BANK112.



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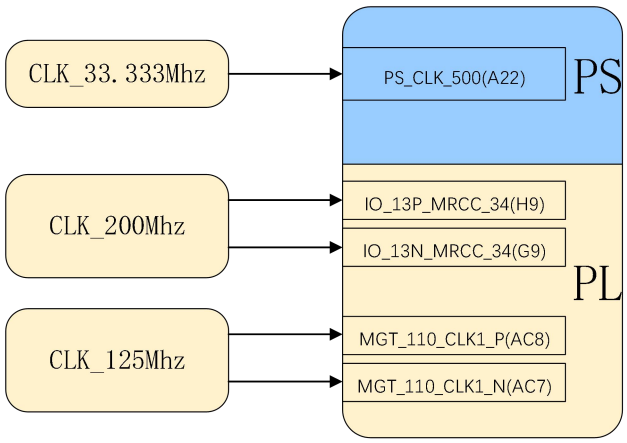
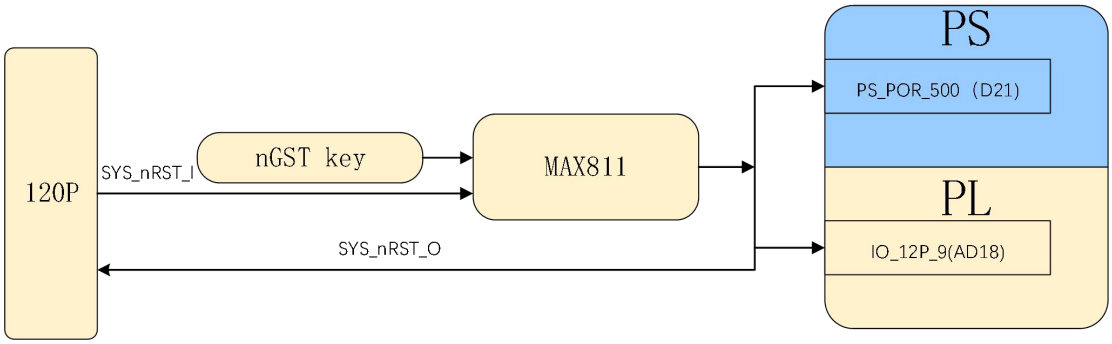



## Part 3.7: Global Reset

**nGST** reset key is provided on the core board, which is the system reset key and is active in low level. This pin also leads to the connector, with the signal name **SYS_nRST_I**, to facilitate the user to add a reset key or design a watchdog reset circuit. At the same time, in order to stabilize the system, we add a reset chip on the core board, and the reset output signal is also led to the connector, the signal name is **SYS_nRST_O**, this signal can be used for the reset of other peripherals on the board, the signal level is 3.3V. The reset pin is shared by **PS/PL** side and is connected to **PS_POR_500** on PS side and **IO_12P_9** (pin position **AD18**) on PL side respectively.

If a reset circuit needs to be designed on the carrier board, the following situations need to be considered.

1) Reset circuit base plate internal use, only need to add reset key and a 0.1uF capacitor parallel port to the ground.
2) The reset circuit should be reserved in structure for external use, and the ground key should be added. At the same time, the 0.1uF capacitor and TVS anti-static device should be connected in parallel to the ground.



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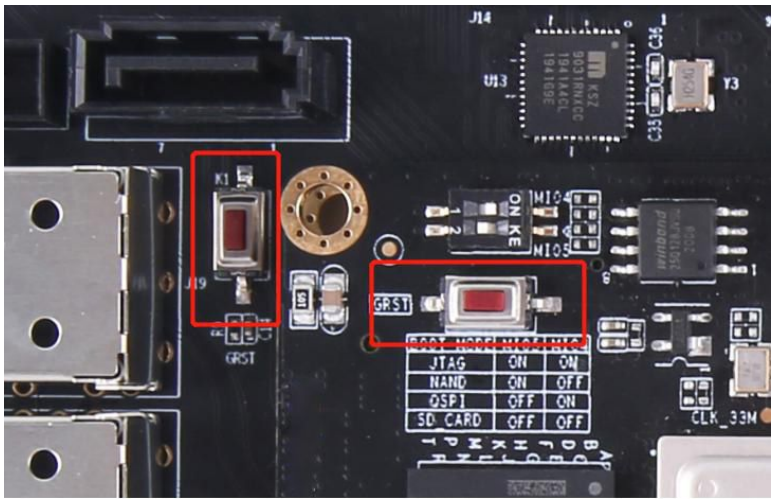
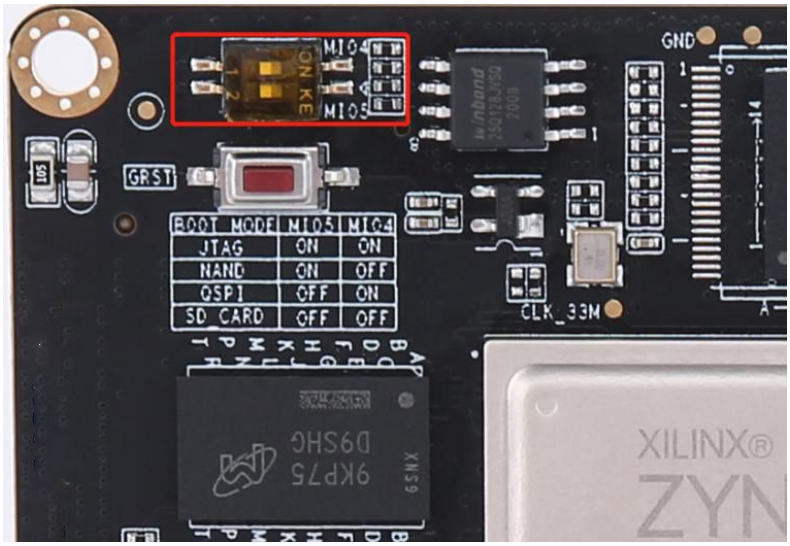



## Part 3.8: Boot Mode Selection

The core board supports four boot modes, namely JTAG, QSPI Flash, NAND, and SD card. The first three modes are installed on the board, and users can realize the SD card mode by connecting on the carrier board. Four startup methods can be selected through the onboard DIP switch. The following figure has listed the position of each mode DIP switch. Due to the high heat output of the main chip, heat sink should be added to the core board, which will block the BOOT MODE selection table.




## Part 3.9: Network Port Connection

The gigabit Ethernet chip is placed on the core board, and the Ethernet chip and ZYNQ chip are connected through the RGMII interface. The corresponding pins are shown in the following table. For Ethernet external connection, only an RJ45 with transformer is required, and the chip address is PHY_AD[2:0]=001

Note: Electrostatic protection should be added to the network port signal cable and LED



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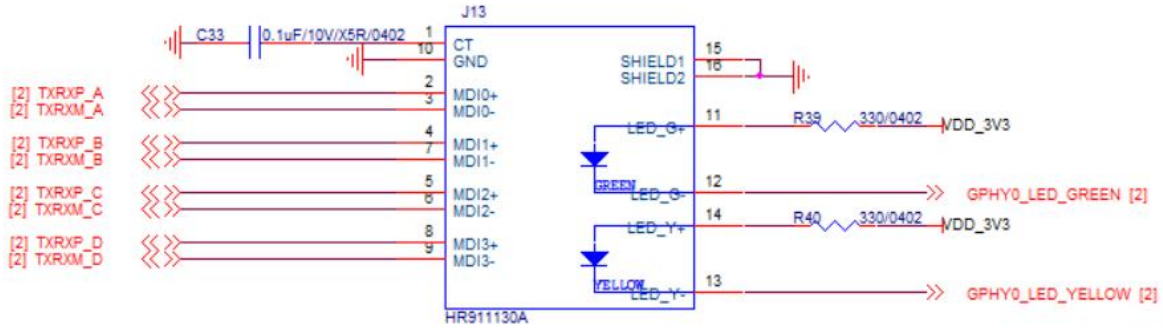
for the product circuit. 2KV or 3KV is used for 0.1uF.

| RMGII Signal | Pin Name | Pin Position |
|---|---|---|
| GTX_CLK | MIO16_501 | L19 |
| TXD0 | MIO17_501 | K21 |
| TXD1 | MIO18_501 | K20 |
| TXD2 | MIO19_501 | J20 |
| TXD3 | MIO20_501 | M20 |
| TX_EN | MIO21_501 | J19 |
| RX_CLK | MIO22_501 | L20 |
| RXD0 | MIO23_501 | J21 |
| RXD1 | MIO24_501 | M19 |
| RXD2 | MIO25_501 | G19 |
| RXD3 | MIO26_501 | M17 |
| RX_CTL | MIO27_501 | G20 |
| PHY_nRST<br>(Power on Reset by Default) | IO_L6P_9 | Y20 |
| MDC | MIO52_501 | D19 |
| MDIO | MIO53_501 | C18 |




## Part 3.10: EMMC Pin Definition

The 8GB EMMC "**THGBMFG6C1LBAIL**" is placed on the FPGA core board, and the operating temperature is -40℃--+85℃. The following table shows the correspondence between the EMMC signal and the ZYNQ pin.

| EMMC Pin | ZYNQ Pin Name | Pin Position |
|---|---|---|
| EMMC_D0 | MIO10 | E22 |
| EMMC_D1 | MIO13 | F22 |
| EMMC_D2 | MIO14 | B22 |
| EMMC_D3 | MIO15 | C22 |
| EMMC_CLK | MIO12 | E21 |
| EMMC_CMD | MIO11 | A23 |



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## Part 3.11: NAND FLASH Pin Definition

NAND FLASH and EMMC adopt compatible designs on the core board. You can only choose one of the two types of welding. You need to specify the welding based on specific requirements.

| FLASH Pin | Pin Name | Pin Position |
|---|---|---|
| DATA0 | MIO5 | C24 |
| DATA1 | MIO6 | D24 |
| DATA2 | MIO4 | E23 |
| DATA3 | MIO13 | F22 |
| DATA4 | MIO9 | A24 |
| DATA5 | MIO10 | E22 |
| DATA6 | MIO11 | A23 |
| DATA7 | MIO12 | E21 |
| RE | MIO8 | C21 |
| CE | MIO0 | F24 |
| CLE | MIO7 | B24 |
| ALE | MIO2 | F23 |
| WE | MIO3 | C23 |
| R/B | MIO14 | B22 |

## Part 3.12: QSPI FLASH

The FPGA Core board has a 32MB QSPI FLASH onboard, the model is W25Q128JVSIQ, which can be used to store startup files and user files. The following table shows the correspondence between QSPI Flash signals and FPGA pins.

| QSPI FLASH Pin | PIN Name | PIN Position |
|---|---|---|
| DATA0 | MIO2 | F23 |
| DATA1 | MIO3 | C23 |
| DATA2 | MIO4 | E23 |
| DATA3 | MIO5 | C24 |
| QSPI_CS | MIO1 | D23 |
| QSPI_CLK | MIO6 | D24 |



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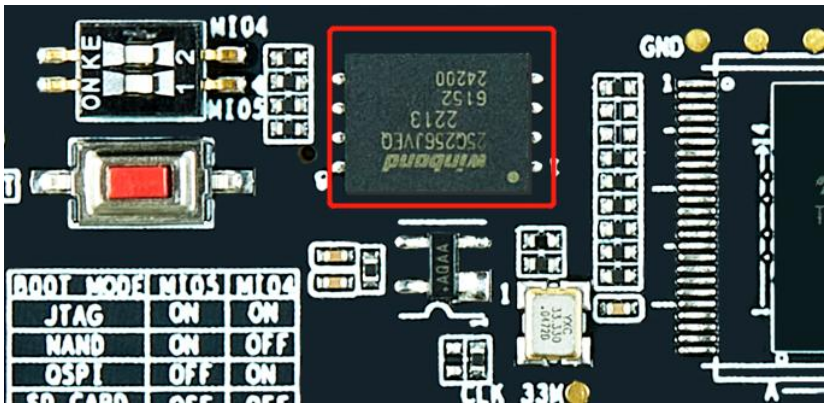

MIO4
MIO5
GND
BOOT MODE | MIO5 | MIO4
JTAG | ON | ON
NAND | ON | OFF
QSPI | OFF | ON
33K

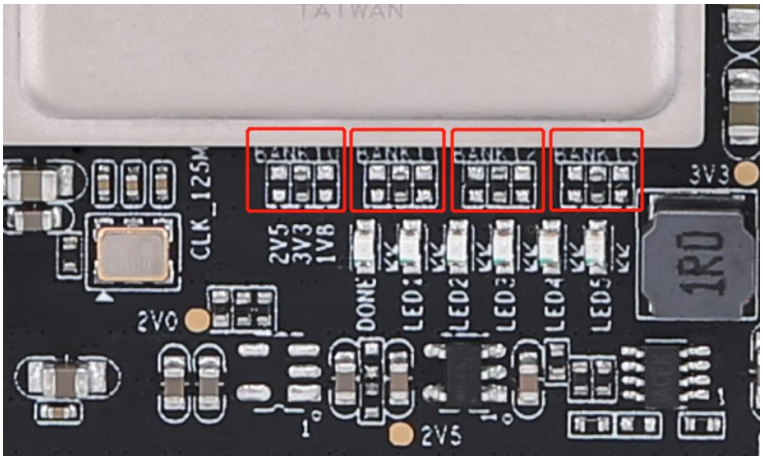
## Part 3.13: On-board LED

In order to facilitate the use of users, five LEDs are placed on the core board, and the pin position of the LED is as follows, when the pin output is high, the LED lights up and the low level LED is off.

| Number | Pin Name | Pin Position |
|---|---|---|
| LED1 | IO-L13N-9 | AA19 |
| LED2 | IO-L14P-9 | AB19 |
| LED3 | IO-L14N-9 | AB20 |
| LED4 | IO-L19P-9 | AD20 |
| LED5 | IO-L19N-9 | AE20 |

## Part 3.14: BANK35 Interface Level Selection

On the COM Core Board BANK35 is HP-BANK, the interface level is fixed to 1.8V, and BANK10/11/12/13 can be soldered with 0 ohm resistance selectors through the instructions provided on the board to achieve three level conversions of 1.8V/2.5V/3.3V. The replacement resistance position is shown below, the order is 2.5V/3.3V/1.8V selected from left to right, and the default soldering 3.3V position, that is, the default interface level of BANK10/11/12/13 is 3.3V.




## Part 3.15: PS Side DDR

The PS side is equipped with two industrial-grade DDR3L chips, a single capacity of 512MB, two total capacity of 1GB, model MT41K256M16TW-107IT:P, DDR3L pin allocation can directly call the system allocation. You can also refer to the routines provided by our company.



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# Part 3.16: PL Side DDR

The PL side is equipped with two industrial-grade DDR3L chips, each with a capacity of 512MB, and the total capacity of the two is 1GB, the model is MT41K256M16TW-107IT:P, DDR3L pin distribution is shown in the following table.

| DDR3L Pin | Pin Name | Pin Position |
|---|---|---|
| DDR3_D0 | IO-L1N-33 | J3 |
| DDR3_D1 | IO-L4N-33 | L2 |
| DDR3_D2 | IO-L1P-33 | J4 |
| DDR3_D3 | IO-L4P-33 | L3 |
| DDR3_D4 | IO-L2N-33 | K1 |
| DDR3_D5 | IO-L6P-33 | K6 |
| DDR3_D6 | IO-L5N-33 | J5 |
| DDR3_D7 | IO-L5P-33 | K5 |
| DDR3_DM0 | IO-L2P-33 | L1 |
| DDR3_DQS_P0 | IO-L3P-33 | K3 |
| DDR3_DQS_N0 | IO-L3N-33 | K2 |
| DDR3_D8 | IO-L11P-33 | H4 |
| DDR3_D9 | IO-L10N-33 | G1 |
| DDR3_D10 | IO-L8P-33 | H6 |
| DDR3_D11 | IO-L7N-33 | F2 |
| DDR3_D12 | IO-L10P-33 | H2 |
| DDR3_D13 | IO-L12N-33 | G4 |
| DDR3_D14 | IO-L8N-33 | G6 |
| DDR3_D15 | IO-L11N-33 | H3 |
| DDR3_DM1 | IO-L12P-33 | G5 |
| DDR3_DQS_P1 | IO-L9P-33 | J1 |
| DDR3_DQS_N1 | IO-L9N-33 | H1 |
| DDR3_D16 | IO-L18P-33 | E1 |
| DDR3_D17 | IO-L17P-33 | E3 |
| DDR3_D18 | IO-L16N-33 | D3 |
| DDR3_D19 | IO-L14P-33 | F4 |
| DDR3_D20 | IO-L18N-33 | D1 |
| DDR3_D21 | IO-L13N-33 | E5 |
| DDR3_D22 | IO-L16P-33 | D4 |
| DDR3_D23 | IO-L17N-33 | E2 |
| DDR3_DM2 | IO-L14N-33 | F3 |
| DDR3_DQS_P2 | IO-L15P-33 | E6 |
| DDR3_DQS_N2 | IO-L15N-33 | D5 |
| DDR3_D24 | IO-L22P-33 | C2 |



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| | | |
|---|---|---|
| DDR3_D25 | IO-L24N-33 | A2 |
| DDR3_D26 | IO-L20N-33 | B4 |
| DDR3_D27 | IO-L20P-33 | B5 |
| DDR3_D28 | IO-L22N-33 | C1 |
| DDR3_D29 | IO-L24P-33 | A3 |
| DDR3_D30 | IO-L19P-33 | C4 |
| DDR3_D31 | IO-L23P-33 | B2 |
| DDR3_DM3 | IO-L23N-33 | B1 |
| DDR3_DQS_P3 | IO-L21P-33 | A5 |
| DDR3_DQS_N3 | IO-L21N-33 | A4 |
| DDR3_A0 | IO-L18P-34 | H7 |
| DDR3_A1 | IO-L21P-34 | L8 |
| DDR3_A2 | IO-L7N-34 | H11 |
| DDR3_A3 | IO-L10N-34 | D10 |
| DDR3_A4 | IO-L15N-34 | H8 |
| DDR3_A5 | IO-L8N-34 | D11 |
| DDR3_A6 | IO-L19P-34 | L7 |
| DDR3_A7 | IO-L10P-34 | E10 |
| DDR3_A8 | IO-L23P-34 | L10 |
| DDR3_A9 | IO-L9P-34 | H12 |
| DDR3_A10 | IO-L18N-34 | G7 |
| DDR3_A11 | IO-L20N-34 | J9 |
| DDR3_A12 | IO-L14P-34 | F9 |
| DDR3_A13 | IO-L7P-34 | J11 |
| DDR3_A14 | IO-L22N-34 | K10 |
| DDR3_BA0 | IO-L22P-34 | K11 |
| DDR3_BA1 | IO-L21N-34 | K8 |
| DDR3_BA2 | IO-L9N-34 | G11 |
| DDR3_CS | IO-L16P-34 | F8 |
| DDR3_RAS | IO-L14N-34 | E8 |
| DDR3_CAS | IO-L17P-34 | E7 |
| DDR3_WE | IO-L16N-34 | F7 |
| DDR3_ODT | IO-L20P-34 | J10 |
| DDR3_RESET | IO-L8P-34 | E11 |
| DDR3_CLK_P | IO-L12P-34 | D9 |
| DDR3_CLK_N | IO-L12N-34 | D8 |
| DDR3_CKE | IO-L17N-34 | D6 |



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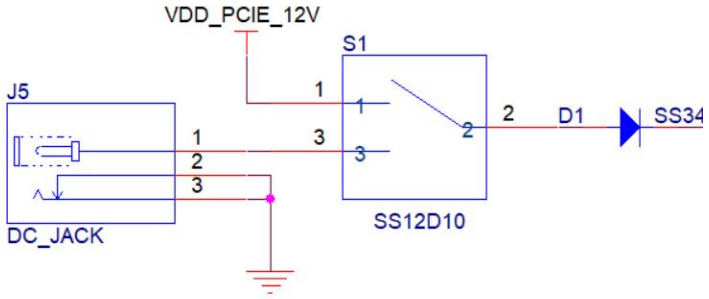
# Part 4: Carrier Board Introduction

## Part 4.1: Power Supply

The FPGA development board provides a 12V/2A power adapter, which can be connected to power the FPGA development board. In addition, the FPGA development board can also provide power through the PCIE interface. After the 12V power supply came in, we used MP2225, MP2143 and AMS1117-1.8 to convert them into 5V/3.3V/1.8V power supply for peripheral use. For the detailed circuit, please refer to the schematic diagram.




## Part 4.2: System Clock

The FPGA development board provides three active clocks for the PS and PL sides. The clock frequency provided by the PS side is 33.333MHz, and the input pin location is PS_CLK_500; the clock frequency provided by the PL side is 200Mhz, and the clock input pin on the PL side is FPGA_13P_MRCC_34/ FPGA_13N_MRCC_34, and the pin location is H9/G9.

The Clock of 33.333MHz and 200Mhz are on the core board.

The GTX section provides a differential 125Mhz clock with the pin name MGT-CLK1P-110/MGT-CLK1N-110 and the pin location AC8/AC7.



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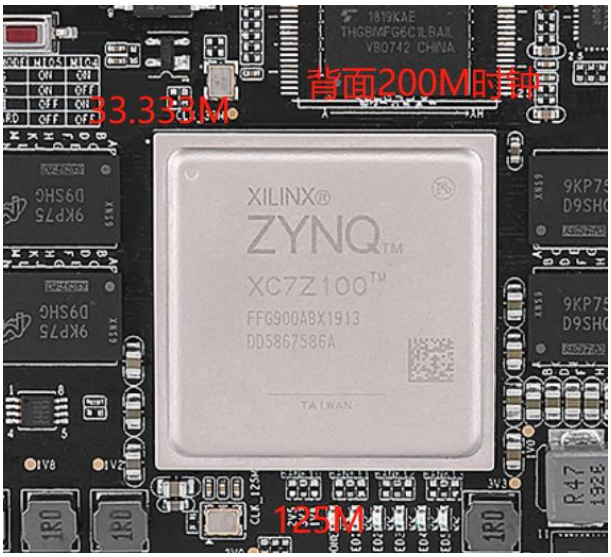
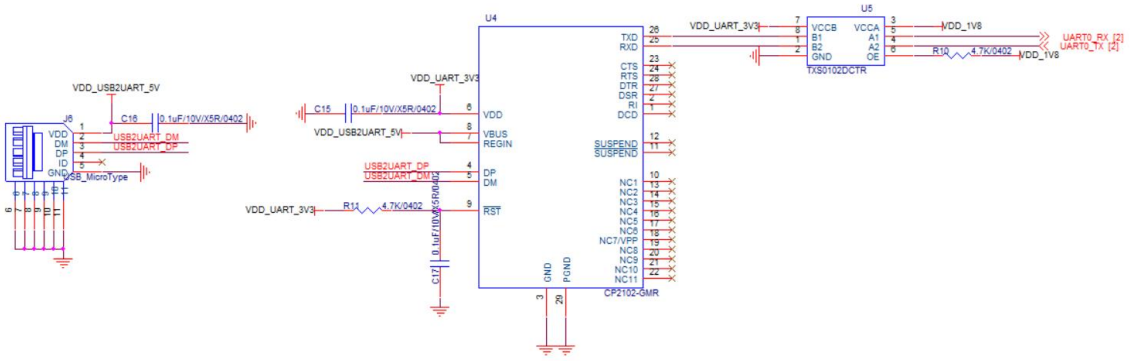



## Part 4.3: USB to UART

The FPGA development board uses Silicon Labs CP2102GM chip to realize USB to UART, and the USB interface adopts Micro USB. Users only need to use a Micro USB cable to connect to the PC for serial communication development. The TX/RX signal of the UART is connected to the BANK501 on the PS side of the ZYNQ, because the level of the BANK501 is 1.8V, but the data level of the CP2102GM is 3.3V, so we use the TXS0102DCUR for level conversion. The following is the signal correspondence table and schematic diagram, the TX/RX direction is defined by the ZYNQ terminal.

| UART0 Pin | ZYNQ Pin Name | Pin Position |
|---|---|---|
| UART0_TX | MIO47 | A18 |
| UART0_RX | MIO46 | F20 |



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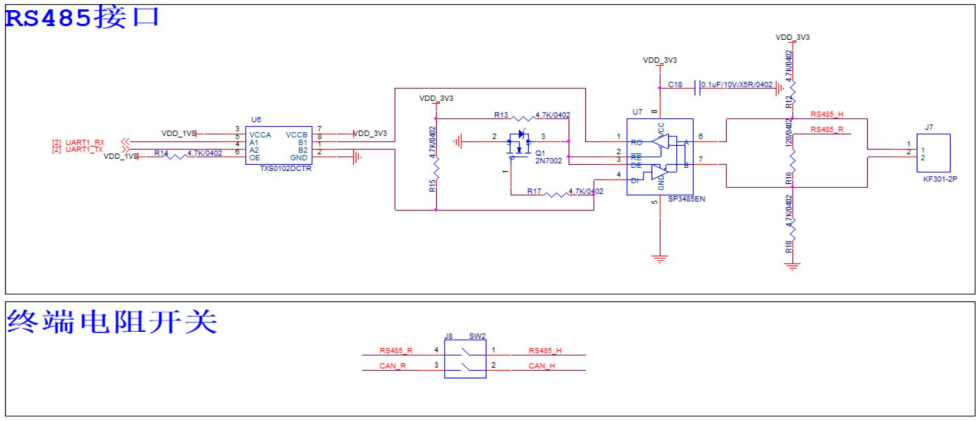
# Part 4.4: RS485 Interface

The FPGA development board uses the "**SP3485**" chip to implement "**RS485**", "**RS485**" external interface adopts 2-pin "**KF301**" connector. The TX/RX signal of "**RS485**" is connected to "**BANK501**" on the PS side of ZYNQ, which is "**URAT1**", because the level of "**BANK501**" is **1.8V**, but the data level of "**SP3485EN**" is **3.3V**, so we use "**TXS0102DCUR**" for level conversion.

In addition, "**RS485**" is a half-duplex communication, and it is necessary to switch the signal direction. This part of Puzhi Electronic Technology has been considered for the user, and the NMOS tube 2N7002 is used to realize the free switching of signal transmission and reception.

The following is the signal correspondence table and schematic diagram, the TX/RX direction is defined by the ZYNQ terminal.

| RS485 Pin | ZYNQ Pin Name | Pin Position |
|---|---|---|
| RS485_TX | MIO48 | C19 |
| RS485_RX | MIO49 | D18 |




# Part 4.5: CAN Bus

The FPGA development board uses the SN65HVD230D chip to implement CAN communication, and the CAN external interface uses a 2-pin KF301 connector. The TX/RX signal of CAN is connected to BANK501 on the PS side of ZYNQ, which is CAN0, because the level of BANK501 is 1.8V, but the data level of SN65HVD230D is 3.3V, so we use TXS0102DCUR for level conversion.

The following is the signal correspondence table and schematic diagram, the TX/RX direction is defined by the ZYNQ terminal.

| CAN Pin | ZYNQ Pin Name | Pin Position |
|---|---|---|
| CAN_TX | MIO51 | F19 |
| CAN_RX | MIO50 | A19 |



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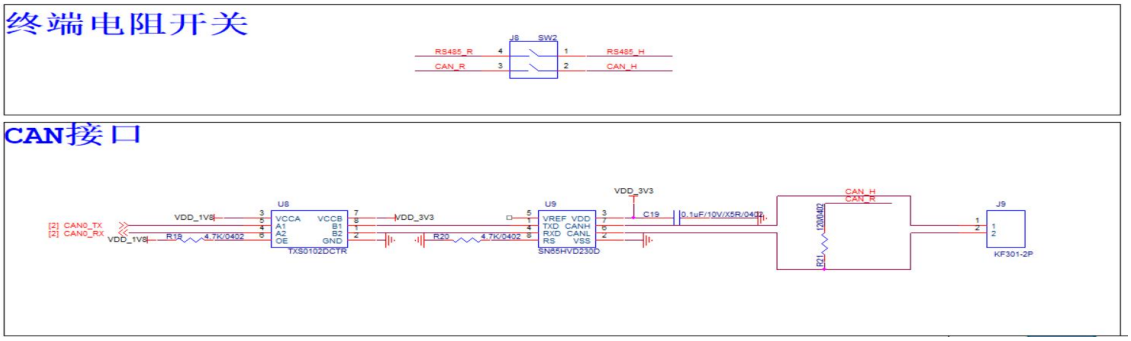
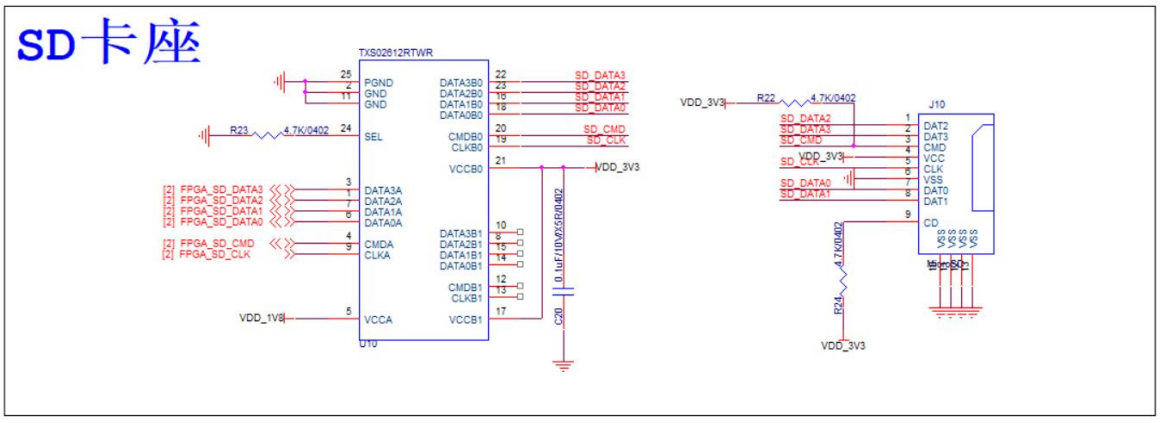



## Part 4.6: SD Card

The SD card holder is placed on the FPGA development board, which is connected to the BANK501 on the PS side of ZYNQ, because the level of BANK501 is 1.8V, but the data level of SD is 3.3V, We use the TXS02612RTWR for level shifting. The following is the pin assignment and schematic diagram of SD card.

| SD Card Pin | ZYNQ Pin Name | Pin Position |
|---|---|---|
| SD_CLK | MIO40 | B20 |
| SD_CMD | MIO41 | J18 |
| SD_DATA0 | MIO42 | D20 |
| SD_DATA1 | MIO43 | E18 |
| SD_DATA2 | MIO44 | E20 |
| SD_DATA3 | MIO45 | H18 |




## Part 4.7: E2PROM

The 64Kbit EEPROM chip is placed on the FPGA development board, the model is AT24C64D-SSHM-T, which is connected to the PL side BANK34 of ZYNQ through the IIC bus. The EEPROM read address is 0xA1, and the write address is 0xA0.

The following is the pin assignment and schematic diagram of the EEPROM.



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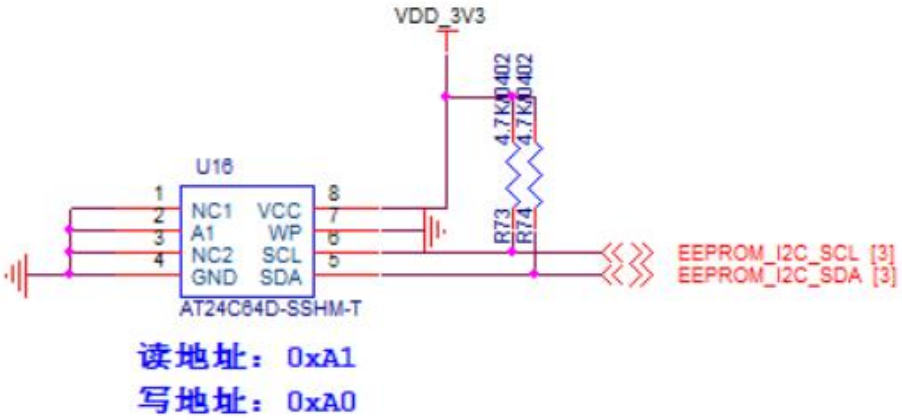
| EEPROM Pin | ZYNQ Pin Name | Pin Position |
|---|---|---|
| IIC_SCL | IO-19P-10 | AC14 |
| IIC_SDA | IO-19N-10 | AC13 |




## Part 4.8: HDMI Interface

The HDMI interface is placed on the FPGA development board. The interface signal is connected to the BANK34 on the PL side of the ZYNQ. For details, please refer to the schematic diagram.

The following is the pin assignment of HDMI, the schematic diagram can be viewed under the folder.

| HDMI Pin | ZYNQ Pin Name | Pin Position |
|---|---|---|
| HDMI_IIC_SCL | IO-11P-13 | U25 |
| HDMI_IIC_SDA | IO-11N-13 | V26 |
| HDMI_DATA0_P | IO-7P-13 | V28 |
| HDMI_DATA0_N | IO-7N-13 | V29 |
| HDMI_DATA1_P | IO-9P-13 | V27 |
| HDMI_DATA1_N | IO-9N-13 | W28 |
| HDMI_DATA2_P | IO-12P-13 | U26 |
| HDMI_DATA2_N | IO-12N-13 | U27 |
| HDMI_CLK_P | IO-23P-13 | U24 |
| HDMI_CLK_N | IO-23N-13 | V24 |
| HDMI_CEC | IO-5P-13 | T29 |
| HDMI_HPD | IO-5N-13 | U29 |
| HDMI_OUT_EN | IO-24P-13 | V23 |



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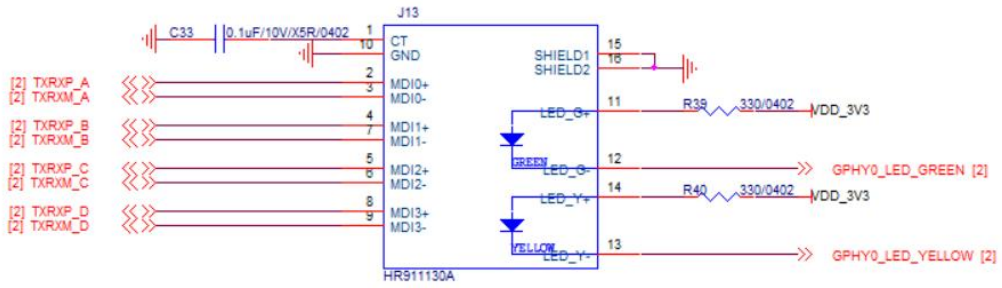
# Part 4.9: Gigabit Ethernet

Two Gigabit Ethernet chips are placed on the FPGA development board. One has been integrated into the core board and is mounted on the PS side, which we define as PHY0; the other is placed on the carrier board and mounted on the PL side, which we define as PHY1. The Ethernet chip and the ZYNQ chip are interconnected through the RGMII interface. PHY0 on the core board only needs to be connected to the RJ45 of the integrated transformer. PHY0 chip address PHY_AD[2:0]=001, refer to the following table for signal connection, and the schematic diagram is as follows. In addition, the reset pin is reserved, and the reset pin of the PHY chip has adopted a power-on reset.

| PHY0 Signal | ZYNQ Pin Name | Pin Position |
|---|---|---|
| GTX_CLK | MIO16_501 | L19 |
| TXD0 | MIO17_501 | K21 |
| TXD1 | MIO18_501 | K20 |
| TXD2 | MIO19_501 | J20 |
| TXD3 | MIO20_501 | M20 |
| TX_EN | MIO21_501 | J19 |
| RX_CLK | MIO22_501 | L20 |
| RXD0 | MIO23_501 | J21 |
| RXD1 | MIO24_501 | M19 |
| RXD2 | MIO25_501 | G19 |
| RXD3 | MIO26_501 | M17 |
| RX_CTL | MIO27_501 | G20 |
| PHY_nRST<br>(Default power-on reset) | IO_L6P_9 | Y20 |
| MDC | MIO52_501 | D19 |
| MDIO | MIO53_501 | C18 |




PHY1 on the Carrier is connected to ZYNQ's BANK35 through RGMII. PHY1 chip address PHY_AD[2:0]=010, signal connection refer to the following table, schematic diagram can refer to the data folder.

| PHY1 Signal | ZYNQ Pin Name | Pin Position |
|---|---|---|
| TX_CLK | IO_16P_35 | D16 |
| TXD0 | IO_8P_35 | G15 |



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| | | |
|---|---|---|
| TXD1 | IO_15N_35 | E17 |
| TXD2 | IO_15P_35 | F17 |
| TXD3 | IO_16N_35 | C16 |
| TX_EN | IO_13N_35 | E15 |
| RX_CLK | IO_13P_MRCC_35 | E16 |
| RXD0 | IO_18P_35 | B17 |
| RXD1 | IO_18N_35 | A17 |
| RXD2 | IO_17P_35 | C17 |
| RXD3 | IO_17N_35 | B16 |
| RX_DV | IO_1N_35 | L14 |
| PHY_nRST | IO_6N_35 | H16 |
| MDC | IO_8N_35 | G14 |
| MDIO | IO_1P_35 | L15 |

## Part 4.10: LEDs

The FPGA development board provides a total of 10 LEDs, 5 LEDs are integrated on the core board, and 5 LEDs are integrated on the carrier board. After the LED pin on the core board outputs a low level, the LED is on, and it is active at a low level. After the LED pin on the FPGA development board outputs a high level, the LED is on, which is active high. The LED colors are all blue. The LED on the core board is mounted on the BANK34, and the LED on the FPGA development board is also mounted on the BANK34.

The pins corresponding to the LEDs are shown in the following table:

| LED Signal | ZYNQ Pin Name | Pin Position |
|---|---|---|
| LED1 (Core Board) | IO_13N_9 | AA19 |
| LED2 (Core Board) | IO_14P_9 | AB19 |
| LED3 (Core Board) | IO_14N_9 | AB20 |
| LED4 (Core Board) | IO_19P_9 | AD20 |
| LED5 (Core Board) | IO_19N_9 | AE20 |
| LED1 (FPGA Board) | IO_3P_10 | AJ14 |
| LED2 (FPGA Board) | IO_3N_10 | AJ13 |
| LED3 (FPGA Board) | IO_11P_10 | AE13 |
| LED4 (FPGA Board) | IO_11N_10 | AF13 |
| LED5 (FPGA Board) | IO_9P_10 | AD14 |

## Part 4.11: KEYs

The FPGA development board provides a total of 5 KEYs, the KEY is pulled up to 3.3V, and the key is low if pressed, that is, the low level is active. The following table lists the connection correspondence of the keys.

| Key Signal | ZYNQ Pin Name | Pin Position |
|---|---|---|
| KEY1 | IO_9N_10 | AD13 |



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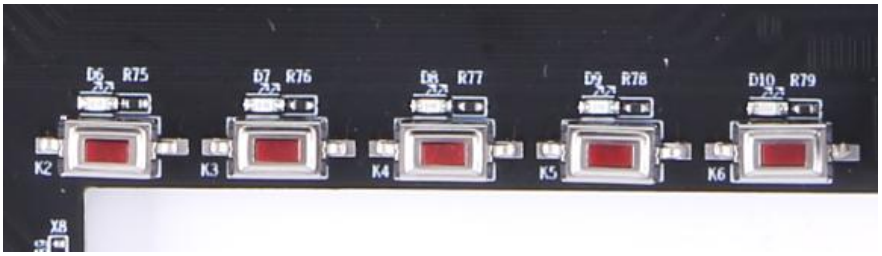
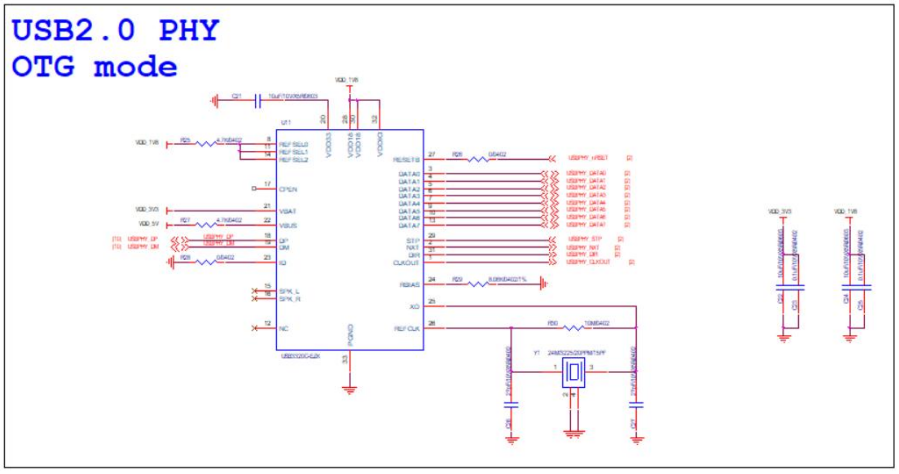
| | | |
|---|---|---|
| KEY2 | IO_21P_10 | AB12 |
| KEY3 | IO_21N_10 | AC12 |
| KEY4 | IO_24P_10 | AB17 |
| KEY5 | IO_24N_10 | AB16 |




## Part 4.12: USB Interface

The FPGA development board is integrated with USB PHY and USB HUB chips to extend 4 USB2.0 main interfaces. The USB PHY needs to be configured into OTG operation mode. The following diagram lists the correspondence between the USB PHY and the main chip. See the development board schematic for details.

| KEY Signal | ZYNQ Pin Name | Pin Position |
|---|---|---|
| USBPHY_DATA0 | MIO32 | K17 |
| USBPHY_DATA1 | MIO33 | G22 |
| USBPHY_DATA2 | MIO34 | K18 |
| USBPHY_DATA3 | MIO35 | G21 |
| USBPHY_DATA4 | MIO28 | L17 |
| USBPHY_DATA5 | MIO37 | B21 |
| USBPHY_DATA6 | MIO38 | A20 |
| USBPHY_DATA7 | MIO39 | F18 |
| USBPHY_STP | MIO30 | L18 |
| USBPHY_NXT | MIO31 | H21 |
| USBPHY_DIR | MIO29 | H22 |
| USBPHY_CLKOUT | MIO36 | H17 |
| USBPHY_nRSET | IO_6P_35 | J16 |



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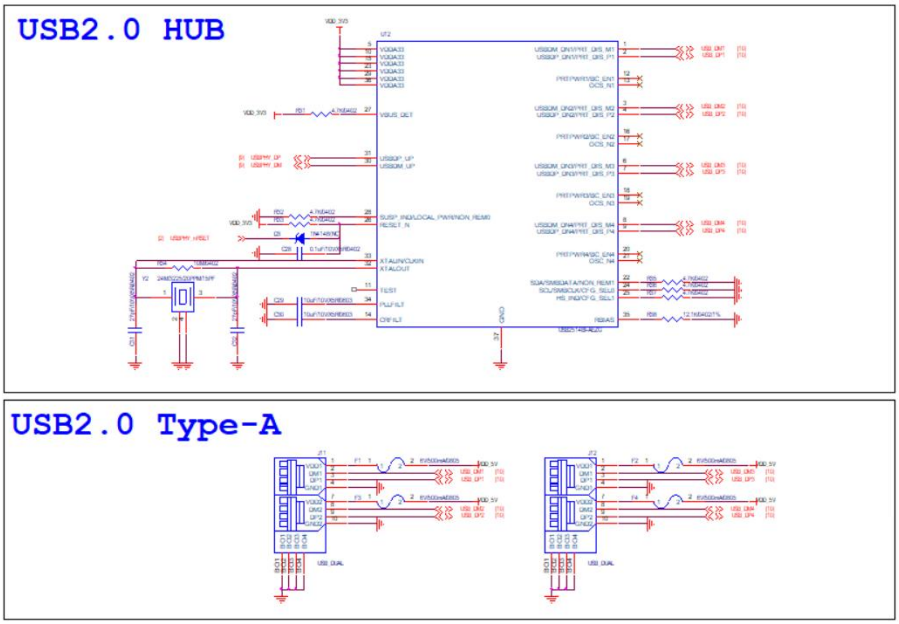


## Part 4.13: SFP Interface

Four SFP interfaces are placed on the FPGA development board, and the ZYNQ7035/7045/7100 supports GTX interfaces up to 10Ghz. The GTX clock is 125Mhz and the input pin names are MGT-CLK1P-110/MGT-CLK1N-110 and the pin locations are AC8/AC7. The following table shows the pin signal correspondence:

| Signal Sequence | ZYNQ Pin Name | Pin Location |
|---|---|---|
| SFP1_TX_P | MGT_111_TX_P3 | V2 |
| SFP1_TX_N | MGT_111_TX_N3 | V1 |
| SFP1_RX_P | MGT_111_RX_P3 | AA4 |
| SFP1_RX_N | MGT_111_RX_N3 | AA3 |
| SFP1_TX_DISABLE | IO_8N_10 | AH13 |
| SFP1_RxRATE_SEL | IO_7P_10 | AE12 |
| SFP2_TX_P | MGT_111_TX_P2 | W4 |
| SFP2_TX_N | MGT_111_TX_N2 | W3 |
| SFP2_RX_P | MGT_111_RX_P2 | Y6 |
| SFP2_RX_N | MGT_111_RX_N2 | Y5 |
| SFP2_TX_DISABLE | IO_7N_10 | AF12 |
| SFP2_RxRATE_SEL | IO_10P_10 | AG12 |
| SFP3_TX_P | MGT_111_TX_P1 | Y2 |
| SFP3_TX_N | MGT_111_TX_N1 | Y1 |
| SFP3_RX_P | MGT_111_RX_P1 | AB6 |
| SFP3_RX_N | MGT_111_RX_N1 | AB5 |
| SFP3_TX_DISABLE | IO_10N_10 | AH12 |
| SFP3_RxRATE_SEL | IO_1P_10 | AK13 |
| SFP4_TX_P | MGT_111_TX_P0 | AB2 |
| SFP4_TX_N | MGT_111_TX_N0 | AB1 |
| SFP4_RX_P | MGT_111_RX_P0 | AC4 |



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| | | |
|---|---|---|
| SFP4_RX_N | MGT_111_RX_N0 | AC3 |
| SFP4_TX_DISABLE | IO_1N_10 | AK12 |
| SFP4_RxRATE_SEL | IO_20P_10 | AA15 |

## Part 4.14: PCIE Interface

The FPGA development board on-board PCIE2.0 interface, is the x8 interface, the following table lists the PCIE interface correspondence.

| Signal Sequence | ZYNQ Pin Name | Pin Location |
|---|---|---|
| PERST_N | IO_20N_10 | AA14 |
| REF_CLK_P | MGT_110_CLK_P0 | AA8 |
| REF_CLK_N | MGT_110_CLK_N0 | AA7 |
| PER0_P | MGT_110_TX_P3 | AD2 |
| PER0_N | MGT_110_TX_N3 | AD1 |
| PER1_P | MGT_110_TX_P2 | AE4 |
| PER1_N | MGT_110_TX_N2 | AE3 |
| PER2_P | MGT_110_TX_P1 | AF2 |
| PER2_N | MGT_110_TX_N1 | AF1 |
| PER3_P | MGT_110_TX_P0 | AH2 |
| PER3_N | MGT_110_TX_N0 | AH1 |
| PER4_P | MGT_109_TX_P3 | AK2 |
| PER4_N | MGT_109_TX_N3 | AK1 |
| PER5_P | MGT_109_TX_P2 | AJ4 |
| PER5_N | MGT_109_TX_N2 | AJ3 |
| PER6_P | MGT_109_TX_P1 | AK6 |
| PER6_N | MGT_109_TX_N1 | AK5 |
| PER7_P | MGT_109_TX_P0 | AK10 |
| PER7_N | MGT_109_TX_N0 | AK9 |
| PET0_P | MGT_110_RX_P3 | AD6 |
| PET0_N | MGT_110_RX_N3 | AD5 |
| PET1_P | MGT_110_RX_P2 | AF6 |
| PET1_N | MGT_110_RX_N2 | AF5 |
| PET2_P | MGT_110_RX_P1 | AG4 |
| PET2_N | MGT_110_RX_N1 | AG3 |
| PET3_P | MGT_110_RX_P0 | AH6 |
| PET3_N | MGT_110_RX_N0 | AH5 |
| PET4_P | MGT_109_RX_P3 | AE8 |
| PET4_N | MGT_109_RX_N3 | AE7 |
| PET5_P | MGT_109_RX_P2 | AG8 |
| PET5_N | MGT_109_RX_N2 | AG7 |
| PET6_P | MGT_109_RX_P1 | AJ8 |
| PET6_N | MGT_109_RX_N1 | AJ7 |
| PET7_P | MGT_109_RX_P0 | AH10 |
| PET7_N | MGT_109_RX_N0 | AH9 |



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# Part 4.15: 40P 2.54mm Expansion Port

The FPGA development board is equipped with three 40P 2.54mm pitch simple horn sockets, which are used to expand the signal connection. BANK35 bit HP BANK, level is fixed at 1.8V. the level of BANK10/11/13 part can be adjusted to 1.8/2.5/3.3V three levels. The following table indicates the chip position where the signal is located. For the detailed connection relationship, please refer to the schematic diagram.

| JM1 Signal Sequence | ZYNQ Pin Name | Pin Location |
|---|---|---|
| 5 | IO_L20P_35 | C12 |
| 7 | IO_L20N_35 | B12 |
| 9 | IO_L2P_35 | J13 |
| 11 | IO_L2N_35 | H13 |
| 13 | IO_L21P_35 | B15 |
| 15 | IO_L21N_35 | A15 |
| 17 | IO_L3P_35 | L13 |
| 19 | IO_L3N_35 | K13 |
| 21 | IO_L24P_35 | A13 |
| 23 | IO_L24N_35 | A12 |
| 25 | IO_L23P_35 | B14 |
| 27 | IO_L23N_35 | A14 |
| 29 | IO_L7P_35 | G17 |
| 31 | IO_L7N_35 | G16 |
| 37 | IO_L5P_35 | K15 |
| 39 | IO_L5N_35 | J15 |
| 6 | IO_L4P_35 | J14 |
| 8 | IO_L4N_35 | H14 |
| 10 | IO_L12P_35 | F15 |
| 12 | IO_L12N_35 | F14 |
| 14 | IO_L14P_35 | D15 |
| 16 | IO_L14N_35 | D14 |
| 18 | IO_L19P_35 | C14 |
| 20 | IO_L19N_35 | C13 |
| 22 | IO_L11P_35 | E13 |
| 24 | IO_L11N_35 | D13 |
| 26 | IO_L10P_35 | F13 |
| 28 | IO_L10N_35 | E12 |
| 30 | IO_L22P_35 | C11 |
| 32 | IO_L22N_35 | B11 |
| 38 | IO_L9P_35 | G12 |
| 40 | IO_L9N_35 | F12 |

| JM2 Signal Sequence | ZYNQ Pin Name | Pin Location |
|---|---|---|



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| | | |
|---|---|---|
| 5 | IO_L19P_13 | P21 |
| 7 | IO_L19N_13 | R21 |
| 9 | IO_L13P_13 | R25 |
| 11 | IO_L13N_13 | R26 |
| 13 | IO_L3P_13 | N28 |
| 15 | IO_L3N_13 | P28 |
| 17 | IO_L4P_13 | N29 |
| 19 | IO_L4N_13 | P29 |
| 21 | IO_L17P_13 | T24 |
| 23 | IO_L17N_13 | T25 |
| 25 | IO_L2P_13 | T30 |
| 27 | IO_L2N_13 | U30 |
| 29 | IO_L22P_13 | U22 |
| 31 | IO_L22N_13 | V22 |
| 37 | IO_L8P_13 | W29 |
| 39 | IO_L8N_13 | W30 |
| 6 | IO_L21P_13 | R22 |
| 8 | IO_L21N_13 | R23 |
| 10 | IO_L18P_13 | P23 |
| 12 | IO_L18N_13 | P24 |
| 14 | IO_L16P_13 | P25 |
| 16 | IO_L16N_13 | P26 |
| 18 | IO_L15P_13 | N26 |
| 20 | IO_L15N_13 | N27 |
| 22 | IO_L20P_13 | T22 |
| 24 | IO_L20N_13 | T23 |
| 26 | IO_L1P_13 | P30 |
| 28 | IO_L1N_13 | R30 |
| 30 | IO_L14P_13 | R27 |
| 32 | IO_L14N_13 | T27 |
| 38 | IO_L6P_13 | R28 |
| 40 | IO_L6N_13 | T28 |

| JM3 Signal Sequence | ZYNQ Pin Name | Pin Location |
|---|---|---|
| 5 | IO_L2P_11 | AK22 |
| 7 | IO_L2N_11 | AK23 |
| 9 | IO_L3P_11 | AJ21 |
| 11 | IO_L3N_11 | AK21 |
| 13 | IO_L15P_11 | AJ20 |
| 15 | IO_L15N_11 | AK20 |
| 17 | IO_L10P_11 | AD21 |
| 19 | IO_L10N_11 | AE21 |
| 21 | IO_L17P_11 | AH19 |
| 23 | IO_L17N_11 | AJ19 |
| 25 | IO_L2P_10 | AH18 |
| 27 | IO_L2N_10 | AJ18 |



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| | | |
|---|---|---|
| 29 | IO_L15P_10 | AF18 |
| 31 | IO_L15N_10 | AF17 |
| 37 | IO_L4P_10 | AJ16 |
| 39 | IO_L4N_10 | AK16 |
| 6 | IO_L24P_11 | AC22 |
| 8 | IO_L24N_11 | AC23 |
| 10 | IO_L18P_11 | AF19 |
| 12 | IO_L18N_11 | AG19 |
| 14 | IO_L23P_11 | AA22 |
| 16 | IO_L23N_11 | AA23 |
| 18 | IO_L16P_11 | AK17 |
| 20 | IO_L16N_11 | AK18 |
| 22 | IO_L20P_11 | W21 |
| 24 | IO_L20N_11 | Y21 |
| 26 | IO_L13P_10 | AG17 |
| 28 | IO_L13N_10 | AG16 |
| 30 | IO_L23P_10 | AC17 |
| 32 | IO_L23N_10 | AC16 |
| 38 | IO_L17P_10 | AE18 |
| 40 | IO_L17N_10 | AE17 |

## Part 4.16: 120P High-Speed Expansion Port

The FPGA development board is equipped with three 120P 0.6mm pitch simple horn sockets, which are used to expand the signal connection. The level of the BANK11/12 section can be adjusted to 1.8/2.5/3.3V, default 3.3V. The following table indicates the chip position where the signal is located. For the detailed connection relationship, please refer to the schematic diagram.

| J23 Signal Sequence | ZYNQ Pin Name | Pin Location | J23 Signal Sequence | ZYNQ Pin Name | Pin Location |
|---|---|---|---|---|---|
| 9 | IO_L5P_12 | AA27 | 10 | IO_L4P_12 | Y28 |
| 11 | IO_L5N_12 | AA28 | 12 | IO_L4N_12 | AA29 |
| 15 | IO_L19P_12 | AH28 | 16 | IO_L6P_12 | AB25 |
| 17 | IO_L19N_12 | AH29 | 18 | IO_L6N_12 | AB26 |
| 21 | IO_L7P_12 | AC26 | 22 | IO_L11P_12 | AB27 |
| 23 | IO_L7N_12 | AD26 | 24 | IO_L11N_12 | AC27 |
| 27 | IO_L21P_12 | AJ28 | 28 | IO_L2P_12 | AB29 |
| 29 | IO_L21N_12 | AJ29 | 30 | IO_L2N_12 | AB30 |
| 33 | IO_L16P_12 | AF30 | 34 | IO_L3P_12 | Y26 |
| 35 | IO_L16N_12 | AG30 | 36 | IO_L3N_12 | Y27 |
| 39 | IO_L20P_12 | AJ30 | 40 | IO_L8P_12 | AD30 |
| 41 | IO_L20N_12 | AK30 | 42 | IO_L8N_12 | AE30 |
| 45 | IO_L10P_12 | AD25 | 46 | IO_L1P_12 | Y30 |
| 47 | IO_L10N_12 | AE26 | 48 | IO_L1N_12 | AA30 |
| 51 | IO_L24P_12 | AJ26 | 52 | IO_L9P_12 | AC29 |
| 53 | IO_L24N_12 | AK26 | 54 | IO_L9N_12 | AD29 |

| | | | | | |
|---|---|---|---|---|---|
| 57 | IO_L14P_12 | AE27 | 58 | IO_L5P_12 | AA27 |
| 59 | IO_L14N_12 | AF27 | 60 | IO_L5N_12 | AA28 |
| 63 | IO_L22P_12 | AK27 | 64 | IO_L12P_12 | AC28 |
| 65 | IO_L22N_12 | AK28 | 66 | IO_L12N_12 | AD28 |
| 69 | IO_L13P_12 | AE28 | 70 | IO_L17P_12 | AG26 |
| 71 | IO_L13N_12 | AF28 | 72 | IO_L17N_12 | AG27 |
| 75 | IO_L18P_12 | AE25 | 76 | IO_L23P_12 | AH26 |
| 77 | IO_L18N_12 | AF25 | 78 | IO_L23N_12 | AH27 |
| 81 | IO_L4P_11 | AJ23 | 82 | IO_L9P_11 | AF23 |
| 83 | IO_L4N_11 | AJ24 | 84 | IO_L9N_11 | AF24 |
| 87 | IO_L1P_11 | AJ25 | 88 | IO_L13P_11 | AG21 |
| 89 | IO_L1N_11 | AK25 | 90 | IO_L13N_11 | AH21 |
| 93 | IO_L6P_11 | AG22 | 94 | IO_L19P_11 | AB21 |
| 95 | IO_L6N_11 | AH22 | 96 | IO_L19N_11 | AB22 |
| 99 | IO_L12P_11 | AE22 | 100 | IO_L14P_11 | AF20 |
| 101 | IO_L12N_11 | AF22 | 102 | IO_L14N_11 | AG20 |
| 105 | IO_L11P_11 | AD23 | 106 | IO_L21P_11 | Y22 |
| 107 | IO_L11N_11 | AE23 | 108 | IO_L21N_11 | Y23 |
| 111 | IO_L7P_11 | AC24 | 112 | IO_L8P_11 | AG24 |
| 113 | IO_L7N_11 | AD24 | 114 | IO_L8N_11 | AG25 |
| 117 | IO_L5P_11 | AH23 | 118 | IO_L22P_11 | AA24 |
| 119 | IO_L5N_11 | AH24 | 120 | IO_L22N_11 | AB24 |



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